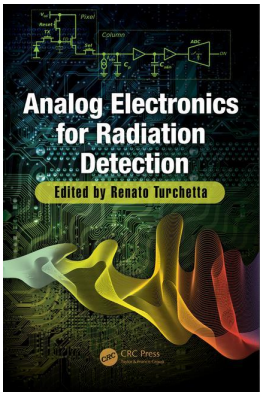

Analog Electronics for Radiation Detection

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3 Analog Electronics for Radiation Detection

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CONTENTS

3.1 INTRODUCTION

This chapter provides guidelines to choose and design analog-to-digital converters (ADCs) for image sensors. Results can be extrapolated to other kinds of radiation detectors on the focal plane. The main architectures usually employed to read out image sensor pixels' outputs are studied and compared. Modern ADC topologies are analyzed. The specific ADC requirements for image sensor applications are also

described. The performance of relevant, recently published ADCs for image sensors is benchmarked. Finally, a discussion of the advantages and disadvantages of the different ADC architectures based on the state of the art is included. A specific figure of merit (FoM) to compare different ADCs for image sensors is proposed. ADCs are widely used for multiple purposes that are related to signal acquisition and data processing. Frame-based image sensors have traditionally included one ADC to read out their outputs and digitize them for further processing, representation, or storage. The image capture is a process with several steps. Image sensors transduce photons into an analog voltage signal that is proportional to the light intensity. Then, this analog output is converted into a digital signal, usually stored on a memory, and sent out for further representation. The quality of the analog-to-digital conversion affects the quality of the final image or frame. Our eyes are quite sensitive to the fixed-pattern noise (FPN) that is introduced during the analog-to-digital conversion. (Humans can detect a 0.5% change in mean intensity [1].) The number of bits of the ADC should be high enough to represent the output image with a number of gray levels that are similar to or higher than the number that our eyes can detect. The speed of the analog-to-digital conversion can limit the frame rate of our sensor. The noise introduced by the ADC should be controlled. Finally, the circuitry in charge of processing the output data flow provided by the converters has to be fast enough to avoid losing information.

Vision sensor designers are not usually experts in the design of ADCs. On the other hand, ADC designers are sometimes not aware of the special requirements that ADCs have to satisfy for image sensors. General-purpose ADCs are not suitable for commercial image sensors. Some of their specifications can be oversized leading to unnecessary power or area consumption. On the contrary, if they do not achieve some of the imager requirements for the signal digitization, they will degrade the image quality.

Traditionally, one global ADC was used to convert all the pixel outputs. ADC designers were not quite concerned about the power and area requirements. However, modern image sensors demand high frame rates and pixels with fine pitch. More than one ADCs are shared by different groups of pixels to increase the readout speed [2]. In this sense, it is crucial to decide how many ADCs are used to convert the pixel outputs, how they are distributed, how the pixel outputs are multiplexed, and the ADC requirements. The specifications of these ADCs can be very different from the converters that are dedicated to communications, for instance.

Emerging three-dimensional (3D) integration technologies also open new, enticing possibilities for ADC design. The conversion speed could be reduced by placing more ADCs in one tier [3]. ADCs could be shared by reduced groups of pixels with a fill factor that is close to 100%. The decision of how many ADCs are going to be placed and how the pixel outputs are going to be multiplexed is not a trivial matter.

The goal of this chapter is to guide image sensor designers to know the specific requirements that ADCs for image sensors must satisfy and how to distribute them and discuss the advantages and drawbacks of the different ADC architectures and topologies. This chapter is organized as follows: first, in Section 3.2, the most common ADC architectures for image sensors are described. Then, in Section 3.3, the

main ADC topologies are analyzed. Next, in Section 3.4, the specific requirements that an ADC for image sensors must satisfy are discussed. Afterwards, in Section 3.5, the state of the art is analyzed, and the performance of relevant ADCs for image sensors is compared. Finally, in Section 3.6, the guidelines for a good choice of an ADC for image sensor applications are given, and the ADC performance of different architectures is compared.

3.2 ADC ARCHITECTURES FOR IMAGE SENSORS

There are four main ADC architectures that are usually employed for image sensor conversion: (1) pipeline, (2) slope (ramp ADCs), (3) cyclic, successive approximation registers (SAR), and (4) sigma delta (ΔΣ). We also find hybrid ADCs that combine the advantages of different architectures. We describe in Sections 3.2.1 through 3.2.5 the principle of operation and advantages and disadvantages of each architecture.

3.2.1 Pipeline ADCs

Pipeline ADCs [4] have a clocked topology with several operation stages. Each stage resolves a certain number of bits of the analog-to-digital conversion. The output of each stage is connected to the next. The m-most significant bits are computed by the first stage, and the rest of the bits are computed by the successive ones. There is the same delay between the output of each stage. Figure 3.1 shows the schematics of a pipeline ADC with m-bit conversion stages. Each stage resolves m-bits and is made up of one m-bit ADC and one m-bit digital-to-analog converter (DAC). Then, the remaining stage output is amplified with a gain $A = 2^m$ and goes to the next stage. Because the bits from each stage are determined at different clock cycles, all the bits corresponding to the same sample have to be time-aligned with shift registers. This imposes area requirements and circuit complexity that limits the usage of these converters with modern column-parallel implementations. They have been employed as global ADCs to read out imager pixel outputs [5]. Its main advantage is high conversion speed. Clock cycles of N_{bits} are required to digitize the input voltage. However, in every clock cycle, the same conversion bits are available from the previous input. The pixel output could be changed after reading the most significant bits of the first conversion stage, adding the possibility of implementing pipeline operation with the pixel readout. Thus, the equivalent pixel conversion speed would be only one clock cycle.

3.2.2 Slope ADCs

Slope ADCs (also known as ramp ADCs) are the most extended converters for image sensors with column-parallel readout topology. Their architecture is rather simple (see Figure 3.2). They have a ramp generator, a comparator, a counter, and an output memory. Initially, the ramp generator and the counter are reset. When the conversion starts, the counter and the ramp generator are activated. If the slope voltage exceeds the input voltage, the counter is stopped, and its outputs are latched. Their

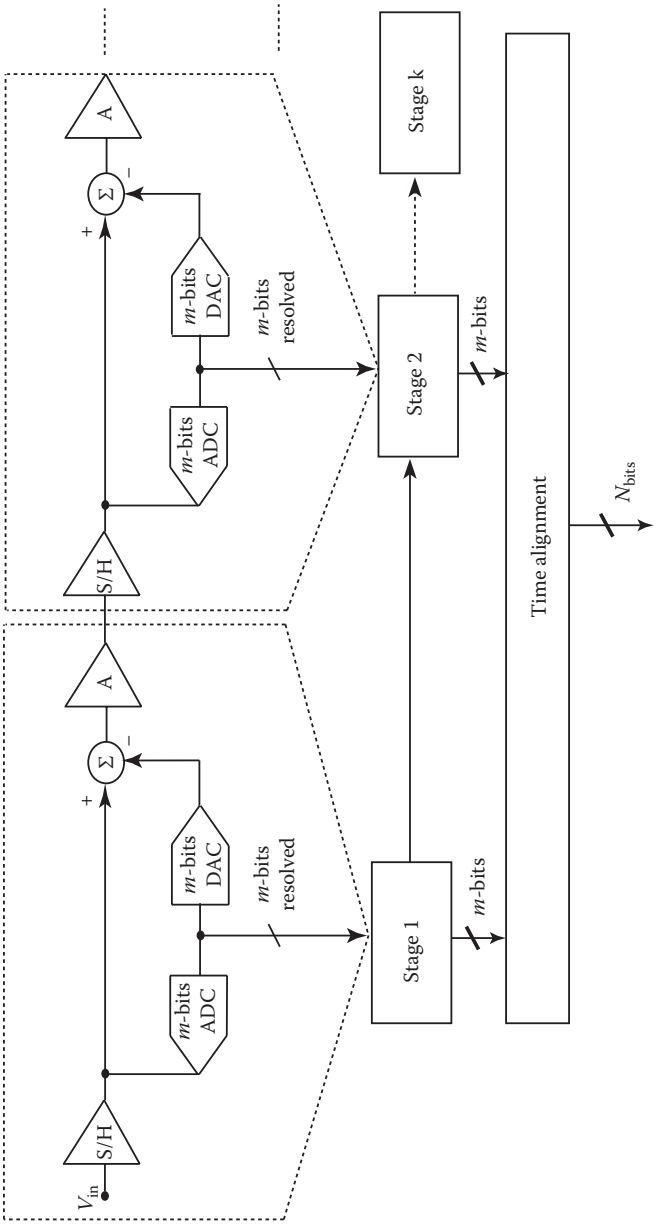

FIGURE 3.1 Pipeline ADC block diagram.

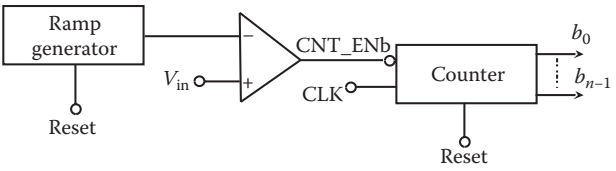

FIGURE 3.2 Ramp ADC block diagram and principle of operation. CLK, counter clock; CNT_Enb, counter outputs enable.

advantages are simplicity, low area requirements (they can be lay out with a fine pixel pitch), and acceptable FPN. Their low area requirements are a great advantage for modern image sensors with a large number of pixels. They can even be embedded inside individual pixels [6] leading to high-speed image sensors.

The main disadvantage of slope ADCs is their conversion speed since $2^{N_{bits}}$ of clock cycles are required to carry out a conversion. Thus, they are more suitable for ADCs with a low bit resolution. To overcome this limitation, several authors propose multiramp ADCs. The input signal is compared to a fast slope to determine the coarse bits of the input signal. Then, a slope with an offset that corresponds to the course of the input signal is activated to determine the less significant bits of the input signal.

There are also some other issues with this architecture: (a) misalignment between coarse and fine conversion ramps and (b) circuit complexity that grows exponentially with the number of coarse-bit conversion. FPN related to ramp ADCs is mainly due to the mismatch of the ramp generators. Ramp generators commonly use capacitors. To improve this limitation, the ramp generators' capacitance is increased. This imposes area requirements to the ADC layout.

3.2.3 SAR ADCs

SAR ADCs overcome the speed limitations of ramp ADCs. SAR ADCs require only N_{bits} clock cycles to perform an ADC conversion. The main limitations of SAR ADCs are area and power consumption. Their principle of operation is as follows (see Figure 3.3): initially, the input analog signal is sampled and held. Then, it is compared to a reference voltage value. The comparison result sets the value of the most significant bit (MSB). Then, the reference voltage is changed, and the comparison is repeated N_{bits}—one time. The control signal end of cell indicates the end of the analog-to-digital conversion. A DAC and digital logic are employed to set the voltage reference values. This imposes expensive area requirements that makes it challenging to implement a SAR for each column. To amend this limitation, it would be possible to share an ADC by a group of pixels. However, in that case, the readout speed requirements would increase. Thus, there is a trade-off between area requirements and speed. Another disadvantage of this kind of converters is the mismatch that is introduced by the DAC. Some authors [7] try to overcome it by calibrating the reference voltage of different DACs. The penalties are more area consumption and circuit complexity. In any case, the DAC design should take into account mismatch considerations to reduce FPN.

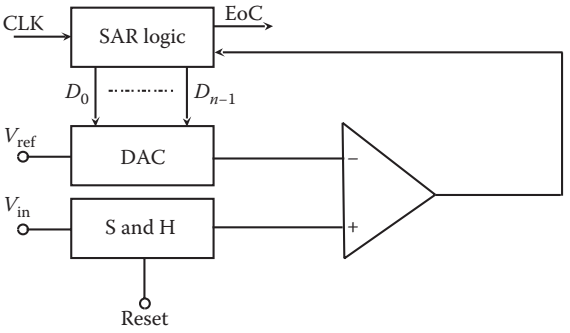

FIGURE 3.3 SAR ADC block diagram.

3.2.4 Cyclic ADCs

The principle of operation of cyclic ADCs is similar to SAR ADCs. They only need N_{bits} clock cycles to operate. The main difference is that the reference voltage, V_{ref}, does not need to be generated during each iteration. Hence, a DAC is not necessary. They employ switched-capacitor (SC) amplifiers, which amplify the difference between the input signal and the reference voltage (see Figure 3.4).

The input signal is changed after each operation cycle. It will be equal to the remaining voltage at the output of the amplifier. After each operation cycle, the remaining input signal is compared to V_{ref} to generate the next MSB. Depending on the value of the MSB, either V_{ref} or zero will be subtracted from the remaining input voltage in the next cycle.

The voltage at the output of the amplifier V_{resout} can be expressed as

$$V_{resout}(k) = A \cdot V_{resin}(k) - d_k \cdot V_{ref} \tag{3.1}$$

where k is the number of the conversion cycle.

Variations of the amplifiers gain can lead to high FPN that can be unacceptable for high-quality image sensors. This imposes a good capacitor matching (more area requirements) and higher currents for the amplifier biasing (more power consumption). FPN and area are the main limitation of cyclic converters for image sensors.

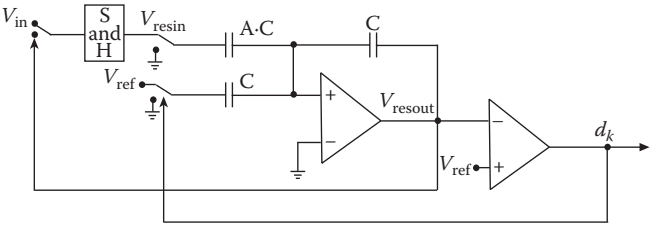

FIGURE 3.4 Cyclic ADC block diagram.

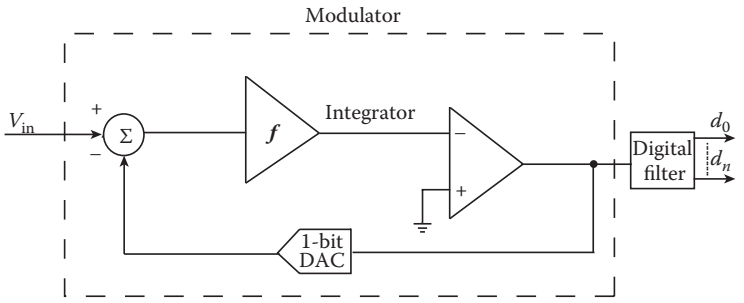

FIGURE 3.5 ΣΔ ADC block diagram.

3.2.5 ΣΔ ADCs

ΣΔ ADCs (see Figure 3.5) have traditionally been used as global ADCs with imagers with low speed and low FPN requirements. They consist of a ΣΔ modulator followed by a digital decimation filter. The modulator has an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The DAC just connects the comparator input to a positive or a negative reference voltage. A clock is necessary to provide the correct timing for the modulator and the digital filter. These kinds of converters suppress the input noise by oversampling. The voltage variations of the input signal are tracked quickly by ΣΔ converters. However, for image sensors with column-parallel readout, it is not necessary to track fast variations of the input signal that can be considered static during the readout process. For this reason, some authors design incremental ΣΔ converters that are optimized to read quasi-static DC signals and negligible offset [8–10].

Their main advantages are low FPN, good resolution, and speed. Their disadvantages are the area requirements, circuit complexity for column-parallel implementation, and their continuous operation mode that can lead to an unnecessary power consumption when they are employed to read out static image sensors' outputs. As it will be discussed in Section 3.6, some of these drawbacks can be solved by adapting the design of ΣΔ converters to the specific requirements of image sensors leading to a very competitive emerging generation of converters.

3.3 ADC TOPOLOGIES

In this section, we are going to discuss the different topologies [2] to digitize pixel outputs. We will study how the conversion speed can be increased by adding more than one ADC per pixel array.

3.3.1 Global ADCs

The traditional approach was to use a single ADC per sensor. All the pixel outputs were time-multiplexed to the input of a global ADC, as shown in Figure 3.6a,

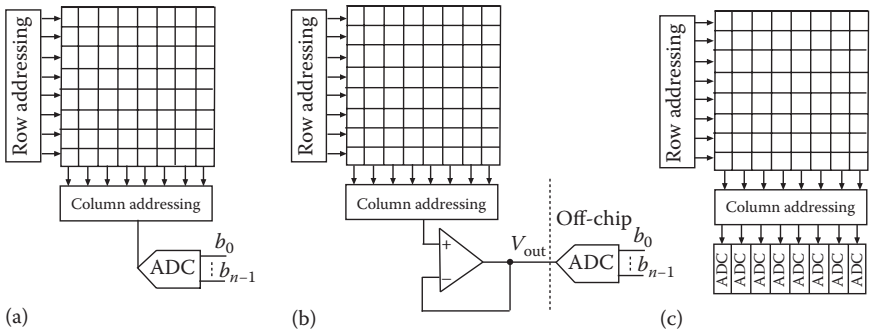

FIGURE 3.6 (a) Readout scheme with a global ADC. (b) Readout scheme with global internal buffer for an external ADC. (c) ADCs in column-parallel distribution.

to provide a digital output. The analog-to-digital conversion frequency of an entire frame is given by the following equation [2]:

$$f_{\text{conv}} = \left[M \cdot N \cdot \left(\tau_{\text{ADC}} + \tau_{\text{RO}} \cdot \frac{n_{\text{bits}}}{n_{\text{parallel}}} \right) \right]^{-1} \tag{3.2}$$

where M and N are the number of pixels per row and column, respectively, τ_{ADC} is the ADC sampling time ($\tau_{\text{ADC}} = 1/f_s$), τ_{RO} is the time that is required to send 1 bit out of the chip, which depends on the master clock frequency, n_{bits} is the number of bits per sample, and n_{parallel} is the number of parallel digital outputs. The ADC was usually integrated on the chip to maximize the frame rate and reduce the FPN. Global ADCs were usually designed to maximize the readout speed. Designers were not very concerned about the area requirements or the power consumption of the ADC. The pixel array area and power consumption were usually much higher than the ADC area and power consumption.

Another approach with a global ADC was to provide an analog readout. The ADC was placed off-chip (see Figure 3.6b). In this case, pixel outputs were first time-multiplexed and then connected to the input of a global internal analog buffer. Analog intermediate memories could also be used to increase the frame rate of the sensor [11]. The internal buffer should be fast enough to guarantee the desired frame rate. It should also be able to provide enough output current to charge or discharge on time the high capacitive load that is introduced by the output pad and the long metal lines.

3.3.2 Column-Parallel ADCs

The demand of commercial sensors with high resolution and high frame rates requires to significantly reduce the time that is dedicated to read out the pixel outputs. Under these requirements, global ADCs are not practical and have been deprecated during the previous years. Obviously, by increasing the number of ADCs working in parallel with different groups of pixels, the frame readout time will be reduced.

For simplicity, by placing one ADC per column (see Figure 3.6c), all the pixels of one row can be sampled and read out simultaneously. This approach has a twofold benefit: the frame readout speed is increased significantly, and the requirements for the conversion time are less restrictive. The frequency of the frame analog-to-digital conversion is almost M times faster:

$$f_{\text{conv}} = \left[M \cdot N \cdot \left(\frac{\tau_{\text{ADC}}}{M} + \tau_{\text{RO}} \cdot \frac{n_{\text{bits}}}{n_{\text{parallel}}} \right) \right]^{-1} \tag{3.3}$$

The main challenges are the area requirements for the ADC. The ADC width should be lower than the pixel pitch. The power consumption should be low because the number of ADCs will be increased significantly. Some authors [12] place one ADC per column alternatively on the top and bottom of the array. Thus, the ADC pitch can be doubled relaxing the ADC area design requirements and achieving the same readout speed than with the column-parallel implementation of Figure 3.6.

It would be even possible to divide the sensor into two blocks and place an ADC per column at the top and bottom of the sensor. The two blocks could be read out in parallel employing a correlated double sampling approach, almost doubling the conversion frequency. This technique is more attractive with pixels with large pitch, typically biomedical arrays with low resolution, where the ADC area and the power requirements are less exigent.

Another issue to take into account with multiple ADCs per sensor is the output data flow. We should have circuitry to store and send out all the ADC outputs. External devices connected to our sensor should also be able to digest the output bit stream.

3.3.3 Pixel-Level Analog-to-Digital Conversion

Some authors [6,13,14] propose digital pixel sensors (DPSs) with integrated ADCs into each pixel. The DPS performance takes advantage of the CMOS scaling-down properties. The idea is simple: each pixel has a dedicated ADC and provides an independent digital output, considerably increasing the readout speed. In this case, the conversion frequency is given by

$$f_{\text{conv}} = \left[\tau_{\text{ADC}} + \tau_{\text{RO}} \cdot M \cdot N \cdot \frac{n_{\text{bits}}}{n_{\text{parallel}}} \right]^{-1} \tag{3.4}$$

Although the conversion speed is higher, there are important drawbacks. This method reduces the pixels' fill factor. It also requires massive parallel circuitry that is capable of reading large amounts of data.

Figure 3.7 compares f_{conv} for the three different readout topologies for different array sizes ($M \cdot N$). We assume for the computation that, $M = N$, $\tau_{\text{ADC}} = 1$ μs, $\tau_{\text{RO}} = 10$ ns, and $n_{\text{bits}} = n_{\text{parallel}} = 12$. These values correspond to standard modern ADC features (see Section 3.5 for more details). The value f_{conv} is always higher using multiple ADCs. For arrays with a low number of pixels, the DPS topologies achieve the

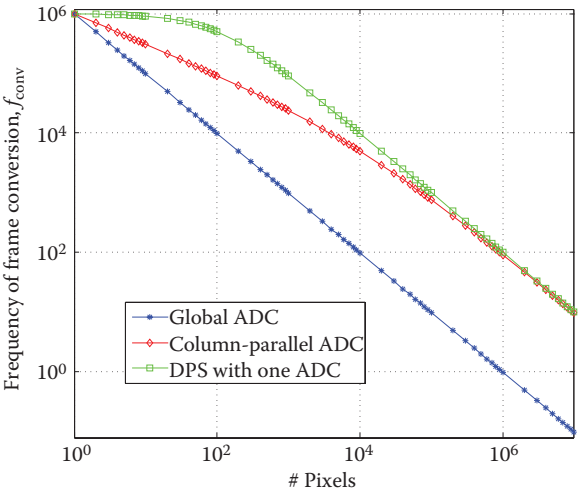

FIGURE 3.7 Frequency of conversion for different ADC topologies: (*) global ADCs, (◇) column-parallel ADCs, and (□) pixel-level ADCs.

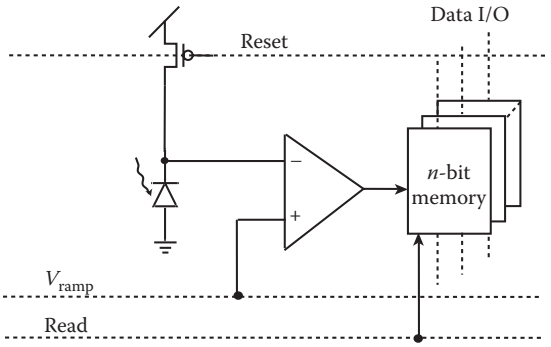

FIGURE 3.8 Diagram of pixel with an internal ramp ADC and *n*-bit digital memory.

highest speed. However, for large-pixel arrays, this topology offers the same performance than the column-parallel topology. For this reason, DPSs are usually aimed for high-speed image sensor applications with low-resolution arrays.

Figure 3.8 shows a DPS with an integrated *n*-bit analog converter. The pixel has an *n*-bit ramp converter and a memory to save its outputs. To reduce the pixel area, some circuitry of the ADCs typically can be shared by the different pixels. In this example, the ramp generator and the counters are shared by all the pixels. Each pixel requires a comparator and a memory to perform the pixel-level analog-to-digital conversion.

3.3.4 Future Integrations

The development of 3D technologies with stacked and interconnected dies opens new possibilities to increase the readout speed without reducing the fill factor. One

entire die (tier) could be dedicated for the ADC design. Ideally, the photoactive area could be placed on the top level, and an ADC per pixel could be placed below it (see Figure 3.9). Kiyoyama et al. recently reported a very interesting ADC for 3D integration [3]. Each pixel block was connected to a dedicated ADC on the bottom tier with a pitch of 100 × 100 μm^2. However, one dedicated ADC per pixel is not feasible with photodiodes with a fine pitch. In this case, it would not be possible to fit an ADC or a processing circuitry below the photodiodes. Thus, the pitch of the processing circuitry will be higher than the photodiode pitch. This implies design challenges to face: (a) groups of photodiodes should share processing circuitry, and (b) they should be multiplexed. Figure 3.10 illustrates a possible implementation with multidistributed processing units (PUs). The pitch of the PUs is bigger than the photodiode pitch. In such topology, f_{conv} is given as

$$f_{conv} = \left[M \cdot N \cdot \left(\frac{\tau_{ADC}}{N_{adc}} + \tau_{RO} \cdot \frac{n_{bits}}{n_{parallel}} \right) \right]^{-1} \tag{3.5}$$

where N_{adc} is the number of ADCs on the bottom tier.

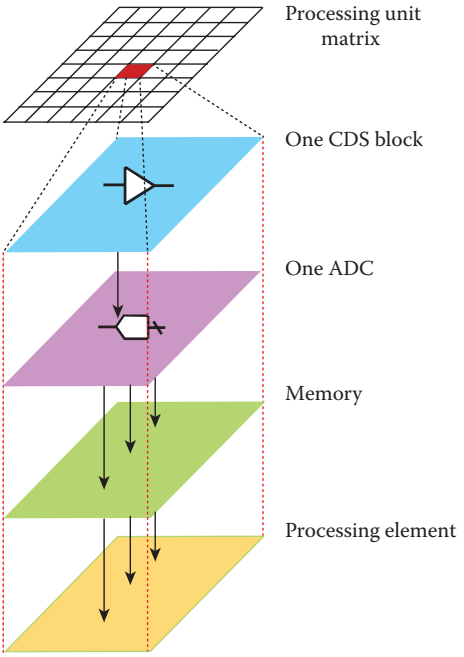

FIGURE 3.9 Diagram of a 3D stacked system with dedicated ADC, memory, and processing elements per pixel. (Adapted from K. Kiyoyama et al., A very low area ADC for 3D stacked CMOS image processing system, *IEEE International 3D Systems Integration Conference, 3DIC*, pp. 1–4, 2011.)

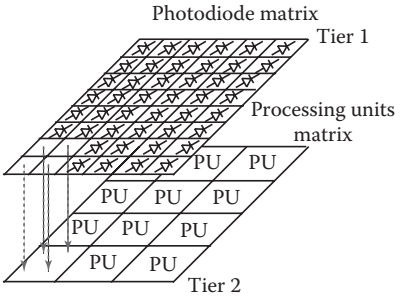

FIGURE 3.10 Possible future 3D integration. Top layer is dedicated to photodiodes. Bottom layer is dedicated to PUs.

3.4 ADC REQUIREMENTS FOR IMAGE SENSORS

In this section, we are going to discuss the specific ADC requirements for image sensors. ADC designers are usually concerned about resolution, speed, and power. As we will discuss, an ADC for image sensors does not need to satisfy strict requirements, but it is desirable to optimize its design to save area and power consumption while maximizing the conversion speed.

3.4.1 ADC Resolution

Figure 3.11 displays an image that is digitized with different numbers of bits. With 4 bits, we clearly notice a loss of image quality for using an insufficient number of bits. With six or more bits, there is not a significative improvement on the image quality. However, a much better resolution is needed to properly capture dark images, when the converter's equivalent input noise is similar to pixel noise. We can wonder how many gray levels our eyes can visualize [15]. There is no clear answer, but several studies have converged that they are roughly 450 under certain illumination conditions. The Digital Imaging and Communications in Medicine (DICOM) standard sets a maximum of 450 gray levels for display representation, for instance. This means that 9-bit resolution is enough for an ADC conversion of the pixel outputs. This is not a very restrictive ADC resolution requirement, taking into account the average bit resolution of the currently reported ADCs. ADCs for image sensors usually employ 10 or more bits.

FIGURE 3.11 Number of bits' effect on image quality. From left to right: 4-, 6-, and 8-bit precision.

The photon shot noise of image sensors can even be exploited to relax the requirements of quantization noise that is introduced by ADCs [16]. Photon shot noise is due to the temporal variations of the number of incident photons. It becomes the dominant noise source with high levels of illumination. Figure 3.12 shows the dependence of a sensor output and various noise sources with illumination. The output has a linear dependence with the illumination level until it saturates at level N_{sat}, which corresponds to the full well capacity of the sensor. Almost all the noise sources are independent of illumination (1/*f* noise, thermal, etc.) and set a noise floor that limits the sensor's dynamic range of operation. However, the photon shot noise depends on the input signal level N_{sig} (number of electrons generated by the photodiode during the integration period) as follows:

$$e_{phs}(N_{sig}) = \sqrt{N_{sig}} \tag{3.6}$$

Photon noise is dominant with bright illumination. We can see that the ADC in this region has less quantization noise than required. Hence, it would be possible to relax the ADC requirements that are related to resolution to reduce the power consumption or increase the speed, for instance.

We can define a quality parameter *r* that is given by the ratio of the quantization noise and the photon noise due to the signal as

$$r = \frac{e_{qns}(k)}{e_{phs}(N_{sig})} \tag{3.7}$$

The quantization noise $e_{qns}(k)$ depends on the quantization step size e_{lsb} and the number of quantization steps *k*, as follows:

$$e_{qns}(k) = k \cdot \frac{e_{lsb}}{\sqrt{12}} \tag{3.8}$$

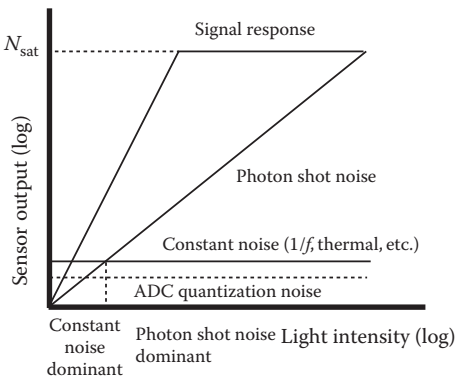

FIGURE 3.12 Dependence of the sensor output and the main noise sources with illumination. (Adapted from M. F. Snoeij et al., *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, 2007.)

For optimal ADC design, the input range of the ADC should be matched to the maximum output swing of the sensor N_{sat}:

$$N_{sat} = 2^n \cdot e_{lsb} \tag{3.9}$$

And, combining Equations 3.6 through 3.9, we can compute the input signal levels at which we can double the quantization noise, i.e., to reduce the ADC resolution to 1 bit, maintaining the ratio between the quantization and the photon shot noise constant:

$$N_{sig} = \left(\frac{k \cdot N_{sat}}{2^n \cdot r \cdot \sqrt{12}} \right)^2 \tag{3.10}$$

Figure 3.13 illustrates how the photon shot noise can be exploited to increase the quantization levels. An elegant design that exploits this property with multiramp ADCs was described by Snoeij et al. [15].

3.4.2 Random Noise

Another feature to take into account is the random noise that is introduced by the converter. It can be expressed in volts, but image sensor designers usually express it in electrons, which is related to the full well capacity of the vision sensor. Random noise provokes column FPN. This is a mismatch that is introduced by the different column ADCs in a column-parallel readout topology. If the different ADCs connected to each column introduce mismatch, we will perceive column variations of the gray levels when the array is illuminated with uniform illumination. As mentioned in Section 3.1, humans can detect a 0.5% change in mean intensity [1]. Therefore, the FPN introduced by an ADC is a very important parameter to take into account for high-quality image sensors. Figure 3.14 illustrates the effect of FPN in a column-parallel readout topology. One captured image with three different levels of FPN is shown. On the right, the

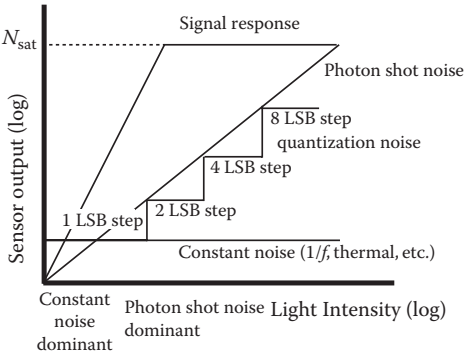

FIGURE 3.13 Illustration of how shot noise can be exploited to relax the ADC quantization noise specifications. (Adapted from M. F. Snoeij et al., *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, 2007.)

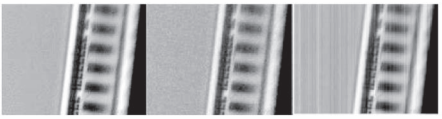

FIGURE 3.14 FPN's effect on image quality.

degradation provoked by FPN on the image is clearly displayed. We observe pixel columns with different gray levels in regions with uniform illumination. This undesirable effect can be improved if the ADCs do not always read the output of the same column in a column-parallel implementation. If the ADC reads out a column that is shifted every time that a different row is selected, the column FPN will be improved.

3.4.3 Area

The area requirements are restrictive for image sensors. If we employ one ADC per column, the ADC pitch must be equal to or lower than the pixel pitch. This limits in many cases the nature of the ADC that we can use. Nowadays, we can find very fine pixel pitches below 1 μm in commercial image sensors. The ADC layout can be very tricky and complicated. Capacitors require a large area to be fitted in a rectangle width that is lower than the pixel pitch. Metal-insulator-metal (MiM), metal-oxide-metal (MoM), and polycapacitors are commonly used to implement SC circuits. Depending on the technology, we can find design rules that limit the pixel pitch.

3.4.4 Speed

The speed of the analog-to-digital conversion is an important parameter to consider. The ADC sampling frequency, $f_s = 1/\tau_{ADC}$, should be higher than

$$f_s \gg \frac{1}{\dfrac{N_{ADC}}{FR \cdot N_{pixels}} - \dfrac{\tau_{RO} \cdot N_{ADC}}{n_{bits}}} \tag{3.11}$$

where FR is the target frame rate, N_{ADC} is the number of ADCs that are shared by all the pixels, τ_{RO} is the amount of time to send 1 bit out the chip, and $n_{parallel}$ is the number of digital outputs. Nowadays, for high-resolution image sensors, usually, $N_{ADC} > 1$. The maximum speed can be achieved when an ADC per pixel is implemented. In that case, all the pixels of the array can be read out simultaneously. Thus, there is a trade-off between readout speed, pixel complexity, and output sensor throughput.

3.4.5 Power Consumption

Since most image sensors are used in mobile devices, power consumption has become an important drawback. Nowadays, the dominant component of power consumption in CMOS image sensors with column-parallel ADCs is analog-to-digital conversion followed by output readout [17,18]. Thus, there is a trade-off between

conversion speed and consumption. Power consumption in CMOS image sensors increases at least linearly in resolution and frame rate.

3.5 STATE OF THE ART

We summarize in Table 3.1 some relevant ADCs that were recently reported in the *IEEE Journal of Solid-State Circuits, IEEE International Solid-State Circuits Conference, VLSI Symposium, IEEE Transactions on Electronic Devices, IEEE Sensors Journal*, and other relevant journals. All of them are targeted for image sensors with parallel readout. They have been tested with pixel arrays of quarter video graphics array (QVGA) resolution or higher. For each converter, we indicate the resolution, the minimum pixel pitch that can be read out, the power consumption, the random noise that is introduced by the converter, the conversion frequency, and the clock frequency of operation.

3.5.1 ADC Efficiency and Design Considerations

Looking at the ADCs for image sensors reported in Table 3.1, we can wonder how efficient they are in terms of energy consumption. There is a theoretic energy that is bound for the sampling energy that is imposed by thermal noise [19]:

$$E_{\min} = 8 \cdot k \cdot T \cdot \mathrm{SNR} = 8 \cdot k \cdot T \cdot 1.5 \cdot 2^{N_{\mathrm{bits}}} \tag{3.12}$$

In Figure 3.15, we have plotted the energy per sample of each converter that is normalized by $E_{\min}$. Murmann [20] established a limit of $E_s/E_{\min} = 100$ for the most efficient current high signal/noise ratio converters, for which energy consumption is just limited by thermal noise (when signal-to-noise and distortion ratio (SINADR) > 60 dB). Looking at Figure 3.15, we see that the most energy-efficient converters for image sensors are still two orders of magnitude above the Murmann's energy limit for modern ADCs. SAR and cyclic converters are more efficient. Slope converters are less efficient and appear on the top of the plot far away from the Murmann's bound. Therefore, the choice of the ADC architecture has an influence on the energy efficiency that should be taken into account.

Figure 3.16 displays the dependency between the ADC resolution and the energy consumption per sample $E_s = P/f_s$. There is an exponential dependency between them. Increasing the bit resolution provokes an exponential increment of the energy consumption. We also have to consider that the total ADC power consumption will be multiplied by the number of columns in a column-parallel implementation. As it was discussed in Section 3.4.1, increasing the ADC resolution does not necessarily improve the image quality beyond nine effective bits. Therefore, limiting the number of effective bits to 10 will save a lot of power.

3.5.2 ADC Comparison

The imager's requirements can be very different depending on the application: surveillance, industrial inspection, video, microscopy, photography, etc. Some applications

TABLE 3.1
Relevant ADCs for Image Sensors Recently Published

Ref.	ADC Type	Resolution	Random Noise	Pixel Pitch	Power	f_s/CLK
[16]	Multiple slope	10b	Adaptive to light intensity	7.5 μm	130 μW	0.8 MS/s/ 20 MHz
[17]	Cyclic	13b	2.5 e^- (153 μV)	5.6 μm	300 μW	19.2 MS/s/ 250 MHz
[18]	ΣΔ	12b	1.9 e^-	2.25 μm	148 μW	0.14 MS/s/ 48 MHz
[21]	Single slope	12b	1.1 e^- (121 μV)	1.4 μm	100 μW	31.7 KS/s/ 130 MHz
[22]	Cyclic with folding integration	13–19b	1.2 e^- (80 μV)	7.5 μm	436 μW	1.5–2.3 MS/s/ 30 MHz
[23]	SAR	14b	2.8 e^- (100 μV)	4.2 μm	41 μW (DC)	3.5 MS/s/ 49.5 MHz
[24]	Single slope	13b	ND	2.5 μm	ND	6.6 KS/s/ 54 MHz
[25]	Single slope	12b	ND	2.97 μm	ND	0.13 MS s/ 2.37 GHz
[26]	ΣΔ + cyclic	14b	ND	3.9 μm	ND	0.125 MS/s/ 5 MHz
[27]	Single/ multiple slope	10b	Adaptive to light intensity	10 μm	ND	0.43–0.047 MS/s/ 49 MHz
[28]	Cyclic	17b	1.17 e^- (21 μV)	7.1 μm	ND	31.15 KS/s/ 1.37 MHz
[29]	SAR	10b	ND	2.25 μm	41 μW	0.56 MS/s/ 7 MHz
[30]	SAR	11b	527 μV	7 μm	209 μW	0.83 MS/s/ 10.8 MHz
[31]	SAR	10b	240 μV	10 μm	35.46 μW	240 KS/s/ 245.76 KHz
[12]	Cyclic	12b	1800 μV	10 μm	430 μW	0.17 MS/s/ 2 MHz
[32]	SS/SAR	11b	1200 μV	3.5 μm	7 μW	0.83 MS/s/ 2 MHz
[33]	SAR	9b	5300 μV	7.4 μm	1.37 μW	33.3 KS/s/ 2.06 MHz
[3]	SAR	9b	335 μV	100 μm (3D integration)	381 μW	4.4 MS/s/ 10 MHz
[9]	ΣΔ	13.5b	70 μV	10 μm (3D integration)	200 μW	46.7 KS/s/ 20 MHz

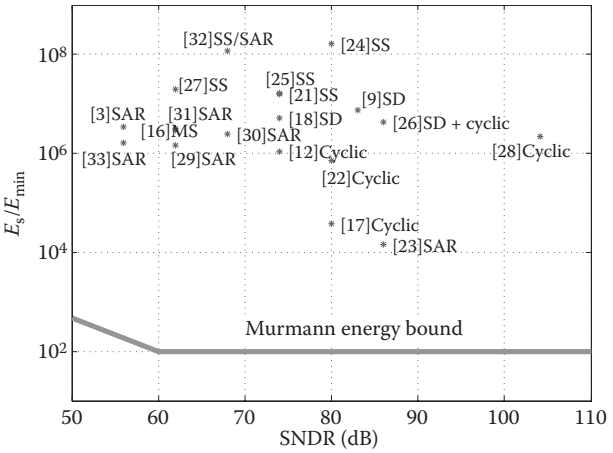

FIGURE 3.15 ADC conversion energy normalized to E_{min} and Murmann's energy bound.

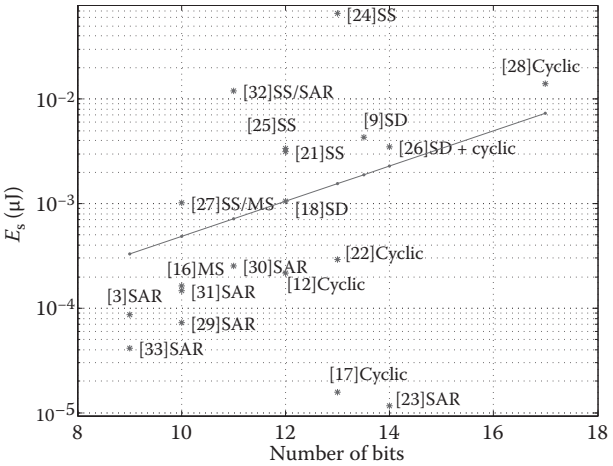

FIGURE 3.16 Energy per sample consumption versus ADC bit resolution. We have plotted in red an exponential data fitting.

require not only low image quality but also low power consumption or high-speed operation (surveillance or industrial inspection), for instance. Others require high image quality (fine pixel pitch) and are less restrictive with operation speed or power consumption, i.e., high-quality imaging. Therefore, ADCs for image sensors should be compared taking into account the scope of application of the imager whose outputs have to be converted. There are specific FoMs to compare ADCs (*International Solid-State Circuits Conference's* FoM, Walden's FoM, Emmert's FoM [34], Jonsson's FoM [35], etc.). However, there are no FoMs for ADCs for image sensors.

In order to compare the performance of the different ADCs for image sensors, we define the following FoM:

$$\text{FoM} = \frac{N_s \cdot \text{pitch}^2 \cdot P}{2^{N_{\text{bits}}} \cdot f_s} \tag{3.13}$$

The FoM was written in the *lower-is-better* form to simplify comparison. It rewards the number of bits, N_{bits}, and the speed sampling frequency, f_s. It penalizes the random noise, N_s, of the ADC (expressed in V_{rms}), the power consumption, P, and the minimum pixel width that can be read out (pitch). As it was discussed in Section 3.4.3, maybe the major design constraint with modern ADC topologies for image sensors is the ADC width (pitch). The required value of the sampling frequency, f_s, should be calculated taking into account the ADC topology, as explained in Section 3.3. The power consumption should be multiplied by the total number of ADCs.

We have compared the column-parallel ADCs of Table 3.1 using the specific FoM that was just defined. Table 3.2 summarizes the FoM values of all the sensors that were reported in Table 3.1. To make the comparison, we assigned the worst reported parameters to the nondisclosed (ND) values of the ADCs that were referenced in Table 3.1.

TABLE 3.2
FoM Values for the ADCs of Table 3.1

Reference	ADC Type	FoM ($\mu J \mu V_{\text{rms}} \mu m^2$)
[23]	SAR	1.26 e – 6
[17]	Cyclic	9.15 e – 6
[28]	Cyclic	1.13 e – 4
[22]	Cyclic with folding integration	1.59 e – 4
[21]	Single slope	1.82 e – 4
[29]	SAR	1.9 e – 4
[18]	ΣΔ	6.88 e – 4
[26]	ΣΔ + cyclic	0.0017
[9]	ΣΔ	0.0026
[30]	SAR	0.0032
[31]	SAR	0.0035
[25]	Single slope	0.0038
[15]	Multiple slope	0.0047
[33]	SAR	0.0220
[24]	Single slope	0.0266
[27]	Single/multiple slope	0.0522
[32]	SS/SAR	0.10
[12]	Cyclic	0.15
[3]	SAR	0.5666

According to this FoM, ramp ADCs [21,24,25] perform worse than SAR or cyclic converters. They are not suitable for high-speed image sensors. For instance, the ramp ADC reported by [25] can operate with conversion rates up to 0.13 MHz, but it needs very fast internal clocks at 2.37 GHz. However, they can be integrated with very fine pitches, and this makes them popular. The SAR ADCs [23,29] offer good performance, with pitches of 4.2 and 2.25 μm, respectively. ΣΔ ADC [18,26] offers a good compromise between all the parameters that we are considering. Finally, cyclic ADCs [17,22,28] score very well with our FoM, but they are limited to pixels with higher pitches than other converters (above 5 μm).

3.6 QUALIFICATION OF DIFFERENT ADC ARCHITECTURES

Although SAR ADCs require a DAC per column, whose area is large for consumer electronics with a fine pixel pitch, they have been adapted and optimized for column-parallel topologies offering very competitive solutions [23,29], according to our FoM. Modern implementations achieve a fine pitch, a good resolution, and a low power consumption.

Cyclic topologies also perform very well according to our FoM. However, cyclic ADCs are less common in commercial column-parallel implementations [17,28]. They are limited to pixels with high pitch. They also require high power consumption. We find interesting and competitive designs in the literature with pixel pitches over 5 μm [17,22]. There are reported hybrid architectures with cyclic converters that exploit some of their advantages [26].

Ramp ADCs score worse with our FoM. However, they can be integrated with very fine pitches and are very frequently used with image sensors [21,24,25]. Their advantages are the low circuit complexity and the low area requirements, with an acceptable noise for image sensors with column-parallel topologies. Their drawback is the low speed because they need faster clocks. According to the most recent, relevant publications in the field of image sensors, ramp ADCs are the most used for their integration in column-parallel structures with a fine pitch. Although they have lower speed than other architectures, their conversion time is enough for the majority of low-speed imaging applications.

ΣΔ converters have been traditionally deprecated and less investigated for column-parallel readout architectures due to their circuit complexity and high area requirements. They usually have been designed for low-noise image sensors, offering lower noise levels and higher speed than ramp converters. Their complexity due to the ΣΔ modulator and the following decimation filters makes it challenging to integrate them with low pitches. However, we find in the literature interesting designs like [18], with a ΣΔ-reduced modulator that is implemented with inverted-based SC circuits, or [26], with a hybrid ΣΔ and cyclic ADC with very low FPN. Specific incremental ΣΔ converters for quasi-static or DC measurements (e.g., imaging or temperature sensors) have also been reported [8–10,36].

3.7 CONCLUSIONS

In this chapter, the advantages and disadvantages of the main ADC architectures for image sensors have been discussed. The special requirements that ADC for image

sensors must satisfy have been defined. We have also presented and compared the frequency of conversion for the main ADC topologies that are suitable for modern commercial sensors. Relevant and recent publications in analog-to-digital converters for image sensors have been reviewed and compared. Moreover, we have defined a specific FoM to compare the different ADCs for image sensors. Finally, the chapter gives guidelines for a good choice of an ADC for image sensors depending on the desired frame rate, the pixel pitch, the noise level that is introduced by the converter, and the target power consumption. Chapter results can be extrapolated to any kind of radiation detector in the focal plane that is made up of a pixel array.

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