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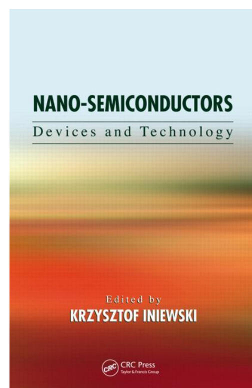

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Facile, Scalable, and Ambient—Electrochemical Route for Titania Memristor Fabrication

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3 Facile, Scalable, and Ambient—Electrochemical Route for Titania Memristor Fabrication

Sumit Chaudhary and Nathan M. Neihart

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3.1 INTRODUCTION

In 1971, using the arguments of symmetry, Leon Chua [1] proposed the existence of a new basic fourth circuit element that he termed the "memristor." Dr. Chua deduced the existence of memristors by examining the mathematical relationships of the four basic electrical quantities (current, voltage, charge, and magnetic flux). As shown in Figure 3.1, these four quantities can be related to each other in six different ways. Two relationships relating magnetic flux (φ) to voltage (v) and charge (q) to current (i) come from basic physical laws (i.e., $d\varphi = v dt$ and $dq = i dt$). The resistor, capacitor, and inductor provide three more relationships by relating voltage to current, voltage to charge, and current to magnetic flux, respectively. Only one relationship remains unaccounted for: the relationship between charge and magnetic flux. A memristor, Chua figured, would relate charge and magnetic flux in a way similar to how a resistor relates to voltage and current. In other words, a memristor will behave like a resistor whose value varies according to the time history of the current passing through the device, and which will remember that value even after the current

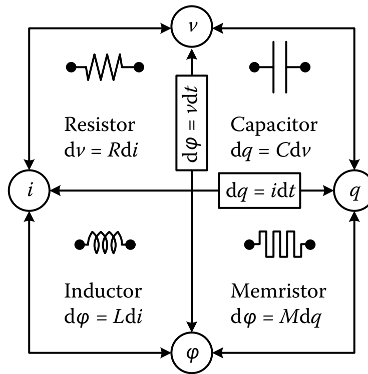

FIGURE 3.1 Four fundamental two-terminal circuit elements: resistor, capacitor, inductor, and memristor.

ceases to flow. In 1976, Chua and Kang [2] generalized the memristor to a family of dynamical systems called memristive systems.

Unfortunately, memristance as a property of a material was, at the time, too subtle to make use of; it was swamped by other effects. The results obtained by Chua [1] were confined to mathematical descriptions and circuit-level macromodels consisting of large numbers of discrete transistors and other passive components. Interestingly however, memristive behavior has been unknowingly observed as far back as the 1960s by researchers in the field of thin-film devices [3, 4]. In the 1960s, relatively thick insulating films of thicknesses greater than 1000 Å were widely used in electrolytic capacitors. Likewise, thin insulating films of thicknesses less than 50 Å had been found to be a powerful tool in the study of superconductivity due to electron tunneling that occurred in such thin films. Hickmott [3] observed that insulating films of medium thickness, that is, thicknesses ranging from 150 to 1000 Å, had not been well studied. Hickmott primarily focused on the study of films made from aluminum oxide and found that in some cases these films would produce an apparent negative differential resistance [3]. What he was unknowingly observing was memristance. For the next 40 years, researchers in the field of thin-film semiconductors would see this same "anomalous" *I–V* characteristic.

In the early 2000s, researchers at Hewlett-Packard, who were working on molecular electronics, began to see the same anomalous *I–V* characteristic behavior in their devices, but recognized it as being memristive. In 2008, Strukov et al. [5] experimentally demonstrated the natural existence of memristance in nanoscale systems where electronic and ionic transports are coupled under an external bias voltage. By fabricating materials that measured mere nanometers in thickness, the memristive behavior of the material begins to be the dominant behavior. Later that year, a physics-based model of the operation of the memristor was also described by Yang et al. [6].

What makes the memristor so radically different from other fundamental circuit elements is its "pinched hysteresis loop," that is, when energized by a sinusoidal voltage, the resulting *I–V* characteristic was a Lissajous curve that cannot be duplicated

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with any combination of resistors, capacitors, or inductors. For this reason, the memristor qualifies as a fundamental circuit element [7]. Moreover, a memristor carries a memory of its past. When the current is disconnected from the circuit, the memristor will remember how much current was applied and for how long.

3.2 THEORY AND DEVICE OPERATION

The most basic mathematical definition of a current-controlled memristor for circuit analysis is the differential form:

$$v = R(w)i \tag{3.1}$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} = i \tag{3.2}$$

where R is a generalized resistance that depends on the state variable of the device, w, which, in this case, is equal to the charge [1]. A more general form of 3.1 and 3.2 was presented in 1976 by Chua and Kang [2] and is given as:

$$v = R(w,i)i \tag{3.3}$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} f(w,i) \tag{3.4}$$

where w can now be a set of state variables and R and f can, in general, be explicit functions of time. Before 2008, even the generalized equations 3.3 and 3.4 were unable to be satisfied by any physical model. In 2008, however, a physical model of a two-terminal device that behaves like a perfect memristor for a restricted range of the state variable, w, was presented [5]. Moreover, if the restrictions on the state variable w are somewhat relaxed, then the model proposed by Strukov et al. [5] shows the more general behavior of a memristive system.

To understand how a memristor works, consider the thin-film semiconductor shown in Figure 3.2. The film consists of a switching medium of thickness D sandwiched between two metal electrodes. The switching medium consists of two

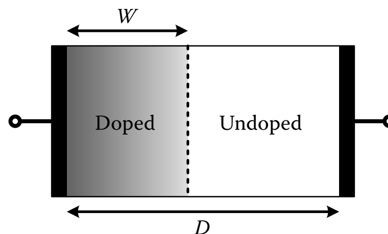

FIGURE 3.2 Schematic representation of memristive operation of a thin-film semiconductor.

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regions, a region of width w with a high concentration of dopants and a region of width $D–w$ with a low concentration of dopants. By applying an external bias voltage across the device, the charged dopants will drift through the switching medium resulting in a shift in the location of the boundary between the high concentration and low concentration of dopants. When the dopants are evenly distributed across the full thickness of the switching medium (i.e., when $w = D$), the total resistance of the film is low and has a value of R_{ON} (Figure 3.3a). When the entire thickness of the switching medium is devoid of dopants (i.e., $w = 0$), the total resistance of the film is high and has a value of R_{OFF} (Figure 3.3b). Therefore, the total resistance of the device can be modeled as a series connection of the two variable resistances, R_{ON} and R_{OFF} as shown in Figure 3.3c [5].

Using the models shown in Figures 3.2 and 3.3c, and considering the simplest case of ohmic conduction and linear ionic drift in a uniform field with an average ion mobility, μ_V, Strukov et al. [5] proposed the following equations that govern the memristance of a thin, semiconductor film:

$$v = \left(R_{ON} \frac{w(t)}{D} R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \tag{3.5}$$

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t) \tag{3.6}$$

which yields the following formula for $w(t)$:

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t). \tag{3.7}$$

By substituting 3.7 into 3.5 and assuming $R_{ON} \ll R_{OFF}$, the memristance of the system, as a function of the charge, can be written as:

$$M(q) = R_{OFF} \left(1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right). \tag{3.8}$$

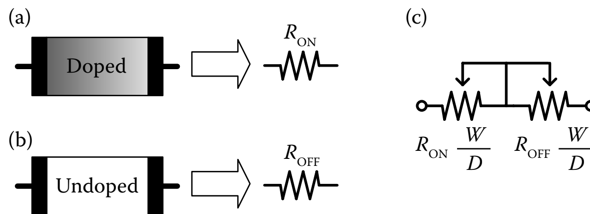

FIGURE 3.3 Schematic representation of a memristor with (a) $w = 0$, (b) $w = D$, and (c) equivalent model of total resistance of the device.

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By considering 3.8, it becomes clear why memristance as a property of the material was not fully observed until recently. The charge-dependent quantity, $\frac{\mu_V R_{ON}}{D^2} q(t)$, in 3.8 is inversely proportional to the square of the thickness of the film, D. This term becomes 10^6 times larger in magnitude as the thickness of the switching medium is reduced from the microscale to the nanoscale, and memristance is correspondingly more significant. Another reason that memristance was hidden for so long was that the original postulation of memristive behavior described by Chua [1] did not account for the boundary conditions of the state variable w, which in this case specifies the distribution of the dopants in the switching medium. In Figure 3.2, it is clear that the variable width of the doped region, w, must be bounded between 0 and D. As shown in 3.7, the state variable w is proportional to the charge q as long as w is less than D. Once w is equal to D, it no longer changes. This condition is referred to as hard switching. Hard switching can occur due to large voltage excursions as well as smaller bias voltages that are applied for long periods [5].

When examining memristive devices, it is important to distinguish them from the more general class of resistive switching devices. Various binary and ternary oxides such as TiO_2, NiO, Nb_2O_5, ZrO_2, or $SrZrO_3$ can be utilized in two-terminal device structures and switched between high and low resistance states by the applications of an appropriate bias voltage [8–12], but not all of these materials result in true memristive behavior. It is necessary to examine the properties that make memristors unique as compared to other types of resistive switching devices. One of the primary differences is in the mechanisms behind the switching from a high resistance state to a low resistance state and vice versa. In the next section, we will examine this difference.

Resistive switching devices (of which the memristor is a subset) can be classified as having either unipolar switching mechanisms or bipolar switching mechanisms. A device that exhibits unipolar switching behavior can be switched from a high resistive state to a low resistive state (and vice versa) using the same voltage polarity. The I–V transfer curves of a unipolar switching device is shown in Figure 3.4a. Bipolar switching, on the other hand, requires voltages of different polarities to switch from the high resistive state to the low resistive state [13] as shown by the

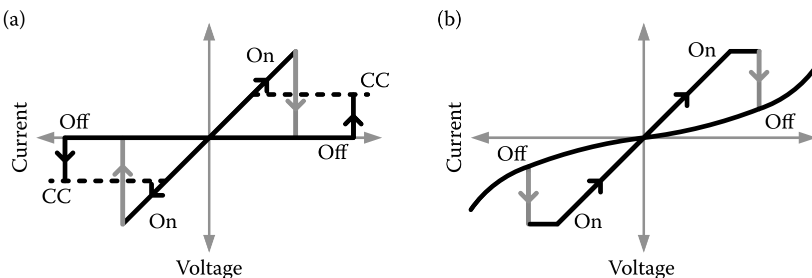

FIGURE 3.4 Voltage–current transfer curves showing (a) unipolar switching and (b) bipolar switching.

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I–V transfer curves in Figure 3.4b. One mechanism for unipolar switching is the fuse–antifuse switching. With fuse–antifuse switching, the low resistance state is achieved through the formation of small conductive filaments between the metal electrodes. The formation of these filaments is initiated by a voltage-induced partial dielectric breakdown in which the material in the discharge filament is modified by Joule heating. Because of the compliance current, only a weak conductive filament with a controlled resistance is formed, which may be composed of the electrode metal transported into the insulator. Once the filament has been formed, the device is in the low resistance state. The high resistance state is then achieved through the destruction of these conductive filaments. This occurs through Joule heating resulting from a high power density on the order of 10^{12} W/cm^3 generated locally, similar to a traditional household fuse but on the nanoscale [13].

Bipolar switching, on the other hand, results from ionic transport. One type of bipolar switching relies on the oxidation of an electrochemically active electrode metal (e.g., silver). The mobile Ag+ cations drift in the ion-conducting layer to discharge at the electrochemically inert counterelectrode leading to a growth of silver dendrites. This forms a highly conductive filament resulting in the switching to the low resistance state. When the polarity of the applied voltage is reversed, an electrochemical dissolution of the conductive filaments takes place, thus switching the device back to the high resistive state [14]. Instead of relying on the migration of cations, a second type of bipolar switching relies on the migration of anions, typically oxygen vacancies, toward the cathode. This type of anion migration is widely believed to be the fundamental switching mechanism in many types of memristors, specifically memristors fabricated out of TiO_2.

This hypothesis was tested in the study of Choi et al. [8], where multiple resistive switching devices were fabricated with a thickness of 57 nm. The bottom electrode on all devices is ruthenium, whereas platinum was used as the top electrode on some of the devices while others used aluminum. The Pt/TiO_2/Ru devices showed resistive switching behavior irrespective of the bias polarity on the platinum top electrode. However, the Al/TiO_2/Ru devices showed switching behavior only when a positive bias was applied to the aluminum top electrode. The reason for this electrode-dependent bipolar or unipolar switching behavior seems to be the oxygen permeation through the top electrode [8]. The thin platinum electrode is well known to have a high oxygen mobility, so that the release of oxygen ions from the TiO_2 to the atmosphere or the incorporation of the oxygen ions from the atmosphere into the TiO_2 interface is fast and active. This is basically due to the nonoxidizing property of platinum, which guarantees easy movement of oxygen ions or atoms along grain boundaries. In contrast, aluminum oxidizes so easily that the permeation of oxygen through the thin aluminum electrode is almost impossible at room temperature. Therefore, when a positive bias voltage is applied to the Al/TiO_2/Ru device, O^{2-} ions in TiO_2 are pulled into the aluminum top electrode resulting in an oxidation of the aluminum and the formation of oxygen vacancies at the TiO_2/Al interface. This hypothesis was verified by wet-etching the aluminum with nitric acid and witnessing aluminum oxide left near the TiO_2 boundary [8].

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The results obtained by Choi et al. [8] with respect to memristors fabricated out of thin films of TiO_2 were later verified by Yang et al. [6] in 2008. In order to more clearly observe the switching mechanisms at work in TiO_2 memristors, a specialized test platform was developed, shown in Figure 3.5. A single crystal substrate of rutile TiO_2 was annealed in 95% N_2 and 5% H_2 gas mixture at 550°C for 2 h to create an oxygen-deficient layer at the surface. Oxygen vacancies in TiO_2 are known to act as n-type dopants, transforming the insulating oxide into an electrically conductive doped semiconductor [15]. As shown in Figure 3.5, two sets of 100 × 100 μm platinum and titanium pads were deposited onto the single crystal. The titanium pads act as a chemically reactive agent to further reduce the TiO_2 to create locally high regions of oxygen vacancies close to the metal/semiconductor interface. The titanium pads were then capped with platinum. Regions in the TiO_2 with oxygen vacancies are denoted TiO_{2-x} in Figure 3.5 [6].

Metal/semiconductor contacts are known to be ohmic if the semiconductor is heavily doped and rectifying in the case of low doping concentrations. The Ti/TiO_{2-x} junction is therefore expected to be ohmic because of the high concentration of oxygen vacancies and the Pt/TiO_2 interface is expected to be rectifying. This was verified by sweeping the voltage between pads 1 and 4 (Figure 3.5) and finding an exponential relationship between the voltage and current as expected with a Schottky rectifier. Sweeping the voltage between pads 2 and 3 (Figure 3.5) showed a linear relationship between the current and voltage, which is expected with ohmic contacts [6].

The investigation found that if a positive bias was applied to pad 3 with pad 4 grounded, the oxygen vacancies migrated to the Pt/TiO_2 barrier eventually forming the low resistance state. Applying a positive voltage to pad 4 at this point will repel the oxygen vacancies back to the titanium contact, thus recovering the high resistance state. This simple experiment demonstrates that anion migration (i.e., bipolar switching) is responsible for the resistive switching in a memristor [6, 14]. To investigate whether the change in the interface is localized (as proposed by Waser and Aono [14]) or uniform, pad 4 was in cut in half and the *I*–*V* relationship was measured from each half of pad 4 to pad 2. Only one of the pad halves showed switching,

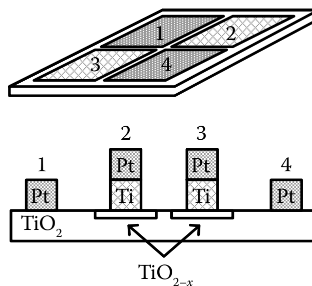

FIGURE 3.5 Test platform used by Yang et al. [6] for investigating switching behavior of memristors fabricated from TiO_2.

demonstrating that conduction is localized instead of uniformly distributed across the entire pad [6].

One important finding by Yang et al. [6] is that switching to the high resistance state is not the result of the rupture of a conduction filament by Joule heating as hypothesized by Waser and Aono [14] (even though the process may be assisted by heat), because the switching observed by Yang et al. [6] was bias polarity–dependent. It is crucial to note that the switching from the low resistance state to the high resistance state occurs at one interface only: the rectifying non-ohmic interface and not the ohmic-like interface. Although the applied voltage bias may also alter the concentration of vacancies at the ohmic interface, the variation is not significant enough to change the ohmic property of this contact for two reasons: the interface has a very large concentration of vacancies to begin with and the electric field there is smaller because of the high conductivity [6]. The non-ohmic interface, however, has a very small concentration of vacancies, and is therefore sensitive to change, and sees a high electric field because of its low conductivity. The two interface junctions are in series, and in such asymmetric devices the total resistance is always controlled by the more resistive non-ohmic interface.

3.3 APPLICATIONS OF MEMRISTORS

Memristors have a wide range of potential applications, and in this section some of the most promising will be discussed. Since the memristor maintains its state, even for zero current, the memristor is a natural candidate for nonvolatile memories [12, 13, 16, 17]. Using the silicon-based memristor that was created for their study, Jo et al. [16] created a memory array capable of storing 1 Kb of data. The memory density was a respectable 2 Gb/cm^2, which is comparable to the memory densities in current DVDs (~2.7 Gb/cm^2). Using Ag/a-Si/p-Si memristive devices (where a-Si is amorphous silicon and p-Si is p-type silicon), the memory demonstrated a yield of 98% and showed programmability for more than 10^5 write cycles.

In addition to memories, memristors are expected to play an important role in extending Moore's law beyond that of simple transistor scaling by obtaining the equivalent circuit functionality using fewer devices or components. One method for achieving this end was proposed by Xia et al. [18], who suggested a way in which memristor-based crossbar arrays can be used to increase the densities of field programmable gate arrays (FPGA). Rather than relentlessly shrinking transistor sizes, Xia et al. [18] separated the logic elements from the data routing network by lifting the configuration bits, routing switches, and associated components out of the complementary metal–oxide–semiconductor (CMOS) layer, and making them part of the interconnect layer. In other words, all of the logic gates in the FPGA are fabricated using a standard CMOS process, and then a post processing step is used wherein a memristor-based crossbar array is deposited on top of the CMOS chip thus serving as a reconfigurable data routing network [18]. The TiO_2 memristor crossbar was integrated on top of a CMOS substrate using nanoimprint lithography and processes that did not disrupt the CMOS circuitry in the substrate.

One advantage of this technique is that a memristor is capable of realizing functions that need several transistors in a CMOS circuit, namely, a configuration-bit

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flip-flop and associated data-routing multiplexor [18]. A further advantage is that their memory function is nonvolatile, which means that they do not require power to refresh their states, even if the power to the chip is turned off completely. Moreover, with appropriate defect-finding and control circuitry, the redundant data paths of the crossbar structure enable alternate routes through the interconnect, resulting in a highly defect-tolerate circuit.

Memristors have also proven very useful in modeling nonlinear systems and researchers have used them to construct efficient circuit models of neurons. Although current digital computers now possess the necessary computing speed and complexity to emulate the brain functionality of animals such as the spider, mouse, and cat [19, 20], the associated energy dissipation grows exponentially along the hierarchy of animal intelligence. For example, to perform certain cortical simulations at the cat scale, even with a neural firing rate 83 times slower than normal, Ananthanarayanan et al. [20] required the use of a super computer equipped with 147,456 CPUs and 144 TB of main memory.

The reason for this huge increase in required computing power is that the brains of biological creatures are configured dramatically differently from the digital computer. The key to the high efficiency of biological systems is the large connectivity (~10^4 in mammalian cortex) between neurons that offers highly parallel processing power. The synaptic weight between two neurons can be precisely adjusted by the ionic flow through them, and it is widely believed that the adaptation of synaptic weights enables biological systems to learn and function.

A synapse is essentially a two-terminal device and bears a striking resemblance to the memristor. Similar to a biological synapse, the conductance of a memristor can be incrementally modified by controlling the charge or flux through it. Jo et al. [21] demonstrated the experimental implementation of synaptic functions in nanoscale silicon-based memristors. In particular, they verified that spike timing–dependent plasticity, an important synaptic modification rule for competitive learning, can be achieved in a hybrid synapse/neuron circuit composed of CMOS "neurons" with memristor "synapses" [21].

The concept of using memristors to model neurons was taken one step further in the study conducted by Pershin et al. [22], where the memristor was used to model the learning behavior of an ameba. Pershin et al. [22] subjected an ameba to a change in temperature and found that the ameba would reduce its movement during a reduction in temperature. Next, they applied a periodic temperature change wherein the temperature was reduced and then allowed to return to normal. It was observed that the ameba would learn the frequency at which the temperature was changing, and once the temperature changes stopped, the ameba would continue to slow its movement in anticipation of the next reduction in temperature. A simple memristor circuit can be used to model the learning behavior of the ameba. In this case, a change in voltage is used to model the change in temperature. Interestingly, it was shown that if the temperature variation was not periodic, or it was interrupted in some way, the ameba (and the memristor-based circuit model of the ameba) would not anticipate future changes in stimulus once the changes stopped [22].

A neural network has also been constructed using a memristor "emulator" [23]. The emulator consisted of a digital potentiometer, and analog-to-digital converter,

and a microcontroller programmed to provide the *I–V* characteristics of a memristor. The neural network was used to demonstrate associative learning and consisted of three neurons, one of each which is used for the sight of food, sound, and salivation. The system was designed such that stimulating the sight neuron resulted in the firing of the salivation neuron. Initially, stimulating the sound neuron did not result in salivation and the goal of this research was to train the memristor-based circuit so that sound would be associated with the sight of food and hence trigger a firing of the salivation neuron [23]. The results showed that this was indeed possible, and much like Pavlov's dog, after the circuit was trained, when the sound neuron was stimulated, the result was a firing of the salivation neuron thereby demonstrating associative learning using a very simple memristor-based circuit [23].

3.4 CURRENT MEMRISTIVE MATERIALS AND FABRICATION TECHNOLOGIES

TiO_2 remains the most studied memristive material system. In TiO_2-based memristors, TiO_2 films are fabricated either by sputter deposition or atomic layer deposition (ALD) with substrate temperature maintained at 200–250°C [18]. To induce oxygen vacancies near the surface of the TiO_2 layer, additional *in situ* annealing in an N_2 environment is performed at 300°C before the deposition of the electrode. For ALD TiO_2 films, titanium (IV) isopropoxide precursor is used with water as the oxidizing agent. Pt is typically used as the metal contact with an adhesion layer of Ti that is a few nanometers thick. Electrodes are deposited using thermal evaporation or electron beam evaporation.

TiO_2 memristors have also been fabricated on flexible substrates using a spin-on sol–gel process that did not require annealing [24]. The procedure consisted of spinning a titanium isopropoxide solution on a flexible plastic substrate, and then leaving the precursor in air for at least 1 h to hydrolyze and form a 60-nm-thick amorphous TiO_2 film. The bottom and the top contacts were aluminum, which was thermally evaporated. For these devices, the operation voltages are less than 10 V, which is a low voltage rate for flexible electronics. They achieved ON/OFF ratios greater than 10,000:1, memory retention of more than 1.2×10^6 s, and reliability after bending the device 4000 times.

Fabrication of TiO_2 memristor nanojunctions and their integration onto CMOS substrates has been achieved [18] using ultraviolet-nanoimprint lithography (NIL) [25]. After finishing the CMOS fabrication, a tetraethyl orthosilicate (TEOS) oxide layer was deposited on top of the chips, which was followed by a chemical mechanical polishing step to expose the tungsten vias. There were two sets of tungsten vias; one set was finally used to address one electrode of the memristors, and the other set was used to address the second electrode. Since the polishing rate of TEOS and tungsten are different, the exposed tungsten vias were a few tens of nanometers below the polished TEOS surface. To alleviate this issue, an extra planarization process was carried out. The surface was made flat by pressing a UV-curable liquid material with a blank quartz plate, and tungsten vias in the CMOS were exposed using photolithography and reactive ion etching (RIE) on the planarized layer. A metal layer was deposited into the holes to the level of the planarized surface, followed by a liftoff in

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acetone. In this fashion, the tungsten vias were brought up to the level of the TEOS, so that they are amenable to connecting with the bottom electrode of memristor nanojunctions to be fabricated using NIL.

The master molds for NIL with nanoscale features (100 nm wide, 100 nm spacing lines of 210 μm long fanning out from grid contact pads) were first fabricated by electron beam lithography and reactive ion etching on a Si substrate with 50-nm-thick thermal SiO_2. The size of the contact pads was 10 × 15 μm, and the pads were composed of grids of 400-nm pitch to assist the flow of the UV-curable resist to obtain a uniform residual layer during imprinting. Daughter molds were duplicated onto optically flat quartz substrates using NIL and RIE. Quartz substrates were chosen because they are transparent to the UV light used in NIL. After the quartz molds were treated with an antisticking layer, NIL was carried out to pattern the bottom electrode on the planarized CMOS substrates with a double layer of resists (transfer layer and UV-curable resist layer on top). After the residual UV resist and the transfer layer were removed by RIE, 9 nm Pt/2 nm Ti bottom electrodes were deposited in an electron beam evaporator at ambient temperature, followed by a liftoff process in acetone. A 36-nm-thick titanium dioxide layer was then sputter coated as the switching material at a substrate temperature of 270°C. The other set of tungsten vias for the top electrodes was exposed and extended in the same fashion, with 120 nm Pt/15 nm Ti layers deposited to extend the tungsten vias to the titanium dioxide surface level using photolithography, RIE, electron beam deposition, and liftoff. Similarly, the top electrodes (12 nm thick Pt) were fabricated using the same processes as for the bottom electrodes. A final photolithography and RIE process was carried out to open the input/output (I/O) pads in the peripheral area, which provided electrical access to the hybrid circuits.

In addition to TiO_2 thin film sandwiched between two electrodes, memristors have also been realized from several other material systems of metal–insulator–metal type configuration. Stewart et al. [26] observed switching and tunable resistance over a 10^2–10^5 range under current and voltage control in organic monolayers sandwiched between planar platinum and titanium metal electrodes. These devices were fabricated by sequential deposition of the bottom electrode, a Langmuir–Blodgett (LB) monolayer, and a top electrode on a flat insulating substrate to form 1 × 1 and 3 × 6 crossbar junction arrays. Three different LB monolayers were investigated: eicosanoic acid deposited as the cadmium eicosanoate salt, an ampiphilic rotaxane, which consists of a mechanically locked dumbbell component and ring component, and the dumbbell-only component of rotaxane. Eicosanoic acid was chosen as the control molecule because it forms well-characterized, highly ordered LB films and is intrinsically an insulator. The rotaxane is representative of a family of molecules that incorporate intrinsic mechanical bistability activated by low voltage reduction–oxidation reactions. The dumbbell-only component of rotaxane was a control for bistable rotaxane. Stewart et al. [12] found that reversible hysteretic switching and resistance tuning was qualitatively similar for all three very different molecular species, indicating a generic switching mechanism dominated by electrode properties or electrode/molecule interfaces, rather than molecule-specific behavior. This report was published in 2004, and upon the discovery of memristors, Williams et al. also included these devices in the class of memristors.

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Jo et al. [16, 27] fabricated a CMOS-compatible memristor using amorphous silicon as the switching medium. The switching occurs in an amorphous silicon device through formation and destruction of a metal filament originating at one of the contacts and piercing into the switching medium. Fabrication of the amorphous silicon layer was done with plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD). Different metals were used for the top contact, and memristive behavior was observed in all cases. Scalability of the devices was also tested down to 50 × 50 nm. The resistance of the "on" state increased by 2.5 times when the device area was reduced by 6 orders of magnitude. Switching speed was also characterized, and 5 ns was generally achieved with the LPCVD devices, whereas PECVD devices saw speeds limited to 150 ns because of higher intrinsic resistance. After programming a state, little degradation of the stored state was seen after more than 5 months at room temperature in ambient air.

Memristive behavior has also been observed in MFe_2O_4 (where M = Mn, Co, or Ni) nanoparticle assemblies [28]. For MFe_2O_4-based memristors, MFe_2O_4 nanoparticles were synthesized using a nonhydrolytic chemical method. The synthesized nanoparticles were coated with organic molecule layers, which can play a role in the electronic transport behavior. Therefore, these organic ligands were removed by sonicating in a basic solution, and nanoparticles were isolated by centrifugation. Isolate nanoparticles were then dried under vacuum at room temperature and nanoparticle assemblies in the form of compact pellets (0.5 × 1 × 4 mm) were made by cold pressing in a die under 160 Pa for 15 min. In order to avoid alteration of the surface properties of the nanoparticles, no heat treatment was used in the preparation of the pellets. The *I–V* characteristics were then probed using a four-point DC method. For assemblies with nanoparticles having sizes below 10 nm, hysteresis was observed in the *I–V* characteristics with an abrupt and large bipolar resistance switching, interpreted by adopting an extended memristor model that combines both time-dependent resistance and time-dependent capacitance.

Memristive behavior has also been observed in other materials such as $SrTiO_3$ [29], NiO [30], V_2O_5 [31], and metallic ferromagnet $La_{0.7}Sr_{0.3}MnO_3$ [32]. In addition to oxygen vacancy–related operation, alternative mechanisms of memristance have also started to appear. For example, in V_2O_5 the memristance arises due to phase transition from an insulator to a metal phase [31]. Existence of spintronic memristors has also been demonstrated in which the memristive operation is based on spin-torque–induced magnetization switching and magnetic-domain-wall motion [33]. Additionally, memristors with an added functionality of light emission have also been demonstrated. This light emitting memristor was fabricated using an ionic transition metal complex ruthenium(II) tris(bibyridine) with hexafluorophosphate counterions [34]. Characterization revealed that not only the current but electroluminescence also exhibited a memory effect. One should note that the number of materials discussed above is not a complete list but covers many of the most primary reports in the literature. In the years to come, it is expected that more materials will be added to the memristor family, in both thin film configuration and nanostructured form, with a variety of operation mechanisms and with more functionalities beyond that of just resistive switching.

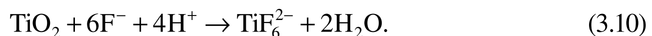
3.5 MEMRISTOR FABRICATION VIA ELECTROCHEMICAL ANODIZATION

Recently, Miller et al. [35] demonstrated memristive behavior in anodic titania, that is, TiO_2 fabricated by electrochemical anodization (oxidation) of Ti. Advantages of the electrochemical route are that the method does not necessarily require high processing temperatures as in the case of sputtering or ALD, and thus the process is more CMOS friendly. Moreover, anodization conditions can be varied in a number of ways, such as changing the anodization time, anodization voltage magnitude waveform, and electrolytic composition, which, in theory, can provide the ability to tune the profile of oxygen vacancies in the resultant oxide. This can enable the tuning of memristive parameters such as threshold voltage, ON/OFF ratio, and frequency response. Moreover, electrochemical anodization can easily be performed on metallic nanostructures, and thus the method is amenable to scaling.

Electrochemical anodization in fluoride-based baths is routinely utilized to form ordered arrays of TiO_2 nanotubes [36]. There are two key processes responsible for anodic formation of nanoporous titania. The first process is the formation of an oxide at the surface of the metal due to the interaction of the metal with O^{2-} and OH^{-1} ions. The anions migrate through the oxide layer reaching the metal–oxide interface where they react with the metal to form an oxide. The equation governing this process can be described as:

$$2H_2O + Ti \rightarrow TiO_2 + 4e + 4H^+. \tag{3.9}$$

The second process is the dissolution of the oxide at the oxide–electrolyte interface due to the Ti–O bond polarization and weakening under an applied electric field. This chemical process can be written as:



$$TiO_2 + 6F^- + 4H^+ \rightarrow TiF_6^{2-} + 2H_2O. \tag{3.10}$$

In the initial stages of anodization, the rate of oxide formation is higher than rate of oxide dissolution. Small pits are formed due to localized dissolution of the oxide, which act as pore forming centers. These pits then convert to bigger pores and the pores spread uniformly over the surface. The pore growth occurs because of the inward movement of the oxide layer due to simultaneous oxide formation and dissolution.

To fabricate memristors using the anodization platform, it was reasoned that anodization time should be small enough so that on a few nanometers of Ti is converted to TiO_2 (memristance being inversely proportional to the oxide thickness) and so that the dissolution process is not yet dominant. The oxide dissolution process will, in fact, be harmful to the memristive device behavior because of the exposure of bare Ti to the top electrode. Our fabrication procedure started with deposition of ~500 nm Ti onto clear glass slides using an electron beam evaporation process. These glass slides were then clamped in an apparatus that exposed about 1 cm^2 circular area of the Ti for anodization. The top half of the apparatus had a hole with an o-ring to hold the electrolyte that would be used for anodization. The electrolyte itself consisted

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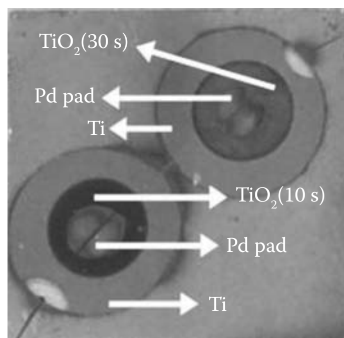

FIGURE 3.6 Photograph of TiO_2 spots on Ti substrate. Anodization for 10 s leads to brown-colored TiO_2 layer (shown in darker gray), and anodization for 30 s leads to blue-colored TiO_2 layer (shown in lighter gray). Different colors are indicative of different thicknesses of TiO_2.

of 0.27 M NH_4 in a mixture of deionized water and glycerol in a volumetric ratio of 16.7:83.3. The anodization was performed at a constant potential of 30 V with the Ti substrate serving as the anode and a platinum mesh dipped in the electrolyte as the cathode. Samples were anodized for 1, 3, 10, and 60 s. Figure 3.6 shows a photograph of two anodized spots with anodization times of 10 and 30 s. The different colors of TiO_2 in the two anodization spots indicate different thicknesses due to different anodization times. The exact thicknesses of the oxide films were not measured, but atomic force microscopy revealed a nonporous nature with sub 100 nm grain sizes (Figure 3.7). In the AFM image of the sample anodized for 60 s, it can be seen that the aforementioned pits have started to appear but pores have not yet formed.

Two sets of identical samples were made. One set was annealed at 550°C for 1 h in an atmosphere of 96% N_2 and 4% H_2 to induce oxygen vacancies on the surface of the TiO_2 layer. The other set was not annealed. This created a total of eight samples, which will be referred to as A1, A3, A10, A60, N1, N3, N10, and N60, where "A" refers to the annealed samples and "N" refers to the nonannealed samples. The numbers 1, 3, 10, and 60 refer to the anodization time of that particular sample in seconds. To create the top contact, palladium was thermally evaporated or dots of silver paste were applied to the newly grown oxide. This created many different testing sites on each sample.

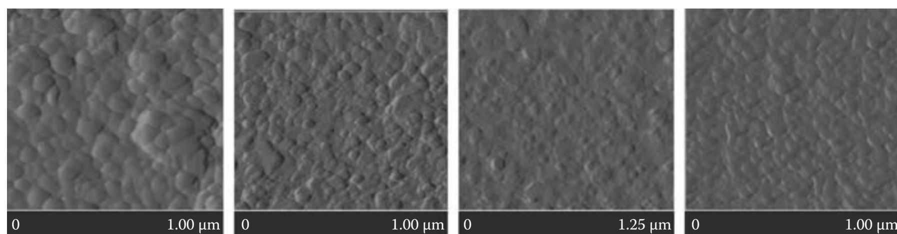

FIGURE 3.7 Atomic force microscopy topography images for non-annealed sample. Left to Right: anodization times of 60 s, 10 s, 3 s, 1 s. Height scale is less than 100 nm for all images.

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3.6 TEST RESULTS OF ELECTROCHEMICAL ANODIZATION-BASED MEMRISTORS

Devices fabricated by electrochemical anodization were characterized using a Keithley 4200 semiconductor characterization system connected to a probe station. The bottom Ti contact was grounded for all measurements. Silver paste or deposited palladium acted as the top metallic contact.

In order to test for memristive behavior in the fabricated devices, each sample was characterized by sweeping the bias voltage from –1 to 1 V and back to –1 V while simultaneously measuring the current. Each sweep consisted of 83 data points taken over approximately 10 s, resulting in 120 ms between each data point. Before the sweep was performed, a forming voltage of 8 V was first applied to each sample. Figure 3.8 shows the results for the nonannealed samples and Figure 3.9 shows the results for the annealed samples. The magnitude of the measured current varies from one sample to the next by as much as 1 order of magnitude. In order to provide a clear comparison between the various samples, the measured current for each sample was normalized by the maximum value for that particular sample.

In Figure 3.8, it can be seen that all nonannealed samples exhibit the bias-dependent bipolar switching characteristics indicative of memristors, as opposed to the filament-controlled unipolar switching characteristics of fuse–antifuse type resistive memory elements [14]. Also, with the exception of sample N60, all samples have a high degree of symmetry with respect to the origin. There are, however, differences in the normalized conductivity of the respective high- and low-conductivity states (referred to as the ON and OFF state, respectively). The normalized conductivity of the ON and OFF state for sample N1 is 890.2 and 61.6 mS, respectively. The normalized conductivity of the ON and OFF state for sample N3 is 1.231 S and 438.5 mS, respectively. The normalized conductivity of the ON and OFF states of sample N10 is 1.2560 S and 22.4 mS, respectively. The conductivity of the ON and OFF state could not be accurately estimated for sample N60 because of the asymmetric nature of the *I*–*V* characteristic.

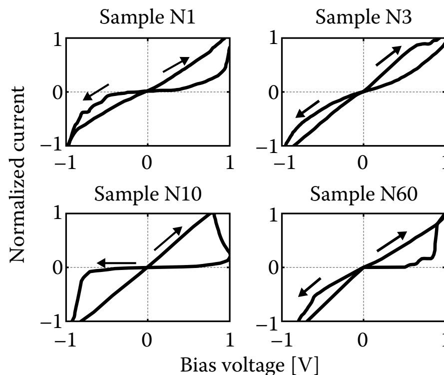

FIGURE 3.8 Memristive switching curves for nonannealed samples N1, N3, N10, and N60. All currents have been normalized. Arrows denote direction of sweep. (© [2010] IEEE.)

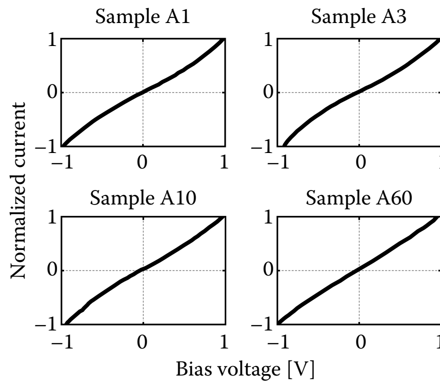

FIGURE 3.9 Current–voltage curves for annealed samples A1, A3, A10, and A60. All currents have been normalized. (© [2010] IEEE.)

The reproducibility of the memristive switching characteristics was also investigated. Figure 3.10 shows three consecutive sweeps for sample N10. The sweep rate was discussed above, and although it was not tested, it is expected that the curves in Figure 3.10 would collapse to resemble the curves in Figure 3.9 if the sweep rate were to be greatly increased. All other nonannealed samples showed similar levels of reproducibility when consecutive measurements were taken at the same spot as well as when measurements were taken at different points on the sample. Slight variations in the current levels across different sweeps, as seen in Figure 3.10, are expected and have been previously observed (e.g., [26]). The current flowing through our memristor is higher in magnitude than previously reported devices (e.g., [5, 6]). However, this is expected because of the larger cross-sectional area of our devices (~1 cm^2 as compared to ~2500 nm^2 for the devices in the report of Yang et al. [6]). Figure 3.9 shows that annealed samples did not exhibit any memristive behavior. *I–V* characteristics for all annealed samples resembled a single ohmic state with a slight

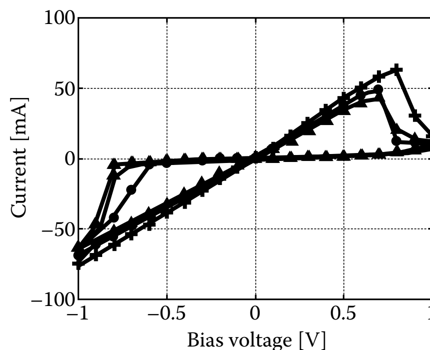

FIGURE 3.10 Current–voltage curves for nonannealed sample N10 showing three consecutive sweeps. (© [2010] IEEE.)

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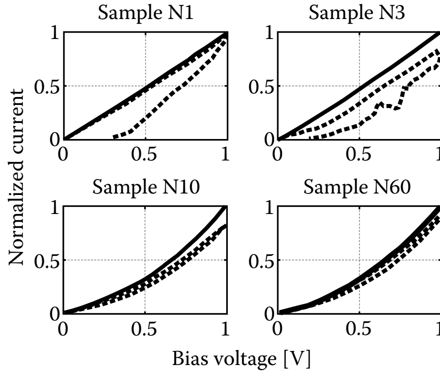

FIGURE 3.11 Soft switching curves for nonannealed samples N1, N3, N10, and N60. All currents have been normalized. Dashed and solid curves represent first and sixth sweeps, respectively. (© [2010] IEEE.)

nonrectifying Schottky barrier nature, as can be seen by a slight deviation of *I–V* characteristics from a straight line.

We also characterized our samples for "soft-switching," the regime in which consecutive bias sweeps of the same polarity lead to changes in conductivity with each sweep [24]. No forming voltage was applied before performing this characterization, and each sweep consisted of 41 data points taking approximately 5 s. The bias voltage for each sample was repeatedly swept from 0 to 1 V and back to 0 V. Figure 3.11 shows the measured curves for the nonannealed samples and Figure 3.12 shows the measured curves for the annealed samples. The dashed and solid curves are the first and last sweep, respectively, in a series of six sweeps.

One possible reason for the superior performance of sample N10 among the nonannealed samples may come from the thickness of the oxide layer. Samples N1 and

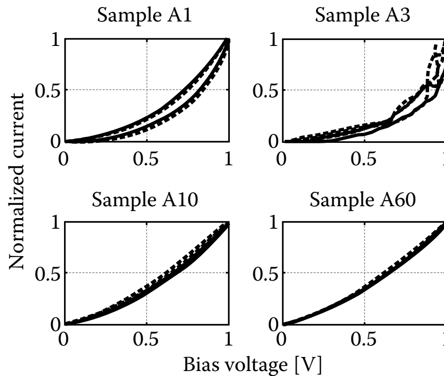

FIGURE 3.12 Soft switching curves for annealed samples A1, A3, A10, and A60. All currents have been normalized. Dashed and solid curves represent first and sixth sweeps, respectively. (© [2010] IEEE.)

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N3 used relatively short anodization times, resulting in thinner oxide layers. It is known that the Ti/TiO_2 interface generates oxygen vacancies [6]. If it is assumed that the quantity of vacancies is roughly equal (because of the equal size of the samples), then as the oxide layer becomes thinner the insulating nature of the oxide degrades and the ON/OFF ratio deteriorates. The reason behind the asymmetry in the *I–V* curve of sample N60 is not clear, but such asymmetries have also been observed by other investigators [6, 24]. Our results show that among the anodization times studied, anodization for 10 s results in the best memristive switching. However, more anodization durations need to be done in order to establish a stronger correlation between memristance and the duration of anodization. Optimal durations are obviously expected to be different for different electrolytes and anodization voltages.

Our understanding of the observed results is as follows. According to the switching mechanism established recently by Yang et al. [6] for metal/oxide/metal type memristors, such memristive devices require one metal/oxide interface to be oxygen vacancy–rich and thus an ohmic contact, and the other metal/oxide interface is required to be a non-ohmic contact. In anodized devices, the bottom Ti/TiO_2 interface is inherently rich with oxygen vacancies. In the case of the annealed samples, extra oxygen vacancies are created at the top of the TiO_2 layer by annealing, in addition to the already existing vacancies at the bottom Ti/TiO_2 interface. This creates ohmic contacts at both terminals, thus leading to the collapse of both memristive switching and soft switching for annealed samples. Thus, annealing is not only not required for anodic TiO_2-based memristors, but is actually detrimental for the devices.

3.7 CONCLUSIONS

After their discovery in 2008, memristors have attracted a lot of interest in the research community, and memristance has been demonstrated in a variety of material systems with TiO_2 being the most widely studied system so far. Although it is generally accepted that bipolar switching, as opposed to unipolar switching, is a primary characteristic of memristive behavior, relatively few circuit-level models of memristors have been proposed in the literature. This will be a major requirement if memristors are to ever become generally adopted by engineers as a new tool for solving engineering problems. Moreover, researchers will need to demonstrate the ability to control the properties of memristive devices such as ON/OFF ratio and frequency response. This will likely come through the discovery of mechanisms for controlling the profile of the oxygen vacancies in the switching medium.

The lack of simple, accurate, time-domain, circuit-level models and tunability, however, has not stopped engineers from beginning to explore potential applications for memristors. Because of their unique nonlinear behavior, memristors have proved useful in a wide variety of applications—from memory elements and flexible signal routing fabrics to the accurate modeling of the operation of neurons and simple single celled organisms.

Perhaps the largest focus in memristor research is currently in the fabrication of devices; TiO_2 has been of particular interest in this regard. TiO_2 films are usually deposited by sputtering and atomic layer deposition methods and then annealed at high temperature to induce oxygen vacancies at the surface of the film. We have

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presented a brief electrochemical anodization of titanium as an inexpensive, simple, and room-temperature alternative for fabricating TiO_2 memristors. It has been demonstrated that no annealing step is required because of the inherent existence of oxygen vacancies at the Ti/TiO_2 interface. Moreover, although it is expected that these devices will show a frequency-dependent, pinched-hysteresis curve, it should be mentioned that this is the only way to definitively prove that the devices are "ideal" memristors, where an "ideal" memristor is one whose input/output relations are described by the time integrals of voltage and current [1, 5].

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