Simulation of Single-Event Effects on Fully Depleted Silicon-on-Insulator (FDSOI) CMOS

Walter Calienes Bartra, Andreas Vladimirescu and Ricardo Reis

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ABSTRACT This chapter is dedicated to single-event effects on fully-depleted silicon-on-insulator (FDSOI) complementary metal oxide semiconductor (CMOS). Circuits using two technological nodes are simulated against heavy-ion impact effects: 32 nm bulk and 28 nm FDSOI. The simulations were done using technology computer-aided design (TCAD) tools.
These devices were used to design six-transistor static random access memory (6T SRAM) cells. These memories were simulated to observe single-event upset (SEU) faults due to heavy-ion impacts in different angles and locations. The 6T SRAM cells designed with FDSOI technology were more resilient against the heavy-ion impacts than the bulk ones.

3.1 Introduction

The continuous scaling of transistors is allowing an increase in the number of components on a chip and also a reduction of voltage values defining a ‘logical’ one. This voltage reduction also makes the circuits more sensitive to radiation effects, as the needed charge to cause a bit to flip is reduced. This chapter presents simulations of single-event effects in fully depleted silicon-on-insulator (FDSOI) transistors and static random access memory (SRAM) cells, comparing these effects with the ones in a traditional bulk complementary metal oxide semiconductor (CMOS) technology. A comparison of resilience with heavy-ion impacts on the drain region between a 32 nm bulk CMOS transistor, a 28 nm FDSOI transistor and a 28 nm high-K FDSOI transistor is presented. The impacts were performed in different transistor locations at different impact angles, whereas previous works considered the impact just at a 0° angle. This comparison was performed with the device in the off state using two-dimensional (2D) technology computer-aided design (TCAD) simulations.

3.2 Fundamentals of the Single-Event Effects

Space and ground environments are reached by a lot of particles created by solar, cosmic or terrestrial activities. These particles can be charged particles (such as electrons, protons or heavy ions) or electromagnetic radiation (such as X-ray and gamma photons). When one of these particles funnels through the silicon die, it loses energy due to an electron–hole pair production. Protons and neutrons can be produced by nuclear reactions, and they can ionise silicon in a similar manner. The particle ionises the silicon in its track, as shown in Figure 3.1. In summary, the basic transient mechanism due to a particle impact can be described in three steps: (1) charge deposition, (2) charge transport and (3) charge collection (Munteanu and Autran, 2008). These phenomena are due to the photocurrents generated in silicon when it is hit by particles or radiation (Calienes and Reis, 2011).

The charges created by particle impact vary with the type of the particle, the hit angle θ and the impact location (Messenger, 1982). These charges
produce an additional transient current $I_p(t)$ and an abnormal charge $Q_p$ in the silicon structure. The model of this transient is summarised in the following equations:

$$I_p(t) = I_0 \exp(-t/\tau_F) - \exp(-t/\tau_R)$$

(3.1)

$$Q_p = I_0 (\tau_F - \tau_R)$$

(3.2)

where $I_0$ is the maximum current due the generated charges, $\tau_R$ is the collection time constant of the junction and $\tau_F$ is the time constant to establish the ion track. Figure 3.2 presents an example of transient current simulation using Equation 3.1, with $I_0 = 350 \mu A$, $\tau_R = 10$ ps and $\tau_F = 100$ ps. The transient
current $I_p(t)$ is maximum when $t = (\tau_F \tau_R \ln(\tau_R/\tau_F))/((\tau_R - \tau_F))$. The terms in Equation 3.1 can be expressed in the following forms (Messenger, 1982):

$$I_0 = q \mu N E_0 \sec(\theta)$$

$$\tau_F = [\mu dE(X)/dX]^{-1}$$

where $q = 1.602 \times 10^{-19}$ C is the electron charge, $\mu$ is the average mobility (which depends on the electric field $E[X]$), $N$ is the electron–hole pair linear density ($\text{cm}^{-1}$), $E_0 = E(0)$ is the electric field at $X = 0$, and $dE(X)/dX$ is the change rate of the electric field with respect to the position. The electron–hole pair linear density depends on the absolute linear energy transfer (LET) in units of megaelectronvolts per centimetre (Holbert, 2012):

$$N = \frac{\text{LET}}{E_{\text{gSi}}}$$

where $E_{\text{gSi}} = 3.6 \text{ eV}$ is the necessary energy to create an electron–hole pair in silicon. LET depends on the particle kinetic energy $E_{\text{kin}}$. The relative LET for a material in $\text{MeV-cm}^2/\text{mg}$ for a particle is defined as

$$\text{LET}_M = \frac{\text{LET}}{\rho_M}$$

where $\rho_M$ is the material volumetric density. In silicon, $\rho_M = \rho_{\text{Si}} = 2329 \text{ mg/cm}^3$. The relative silicon LET is also expressed in other units as picocoulombs per micrometre ($1 \text{ pC/\mu m} = 96.525 \text{ MeV-cm}^2/\text{mg}$) (Naseer, 2008).

Table 3.1 shows the principal sources of natural space radiation (Ecoffet, 2007). These radiations can reach the earth. Other radiation sources include the manufacturing materials used in the fabrication of integrated circuits (Wrobel et al., 2009).

In the literature, the faults due to particle impacts are known as single-event effects because they are due to a single particle or heavy ion. The single-event effects have subcategories (Boudenot, 2007), such as

- Single-event transient (SET): Transient fault in combinational circuits
- Single-event upset (SEU): Transient fault in sequential circuits and memories

<table>
<thead>
<tr>
<th><strong>TABLE 3.1</strong></th>
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<tbody>
<tr>
<td><strong>Main Sources of Natural Space Radiation</strong></td>
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<tr>
<td><strong>Radiation belts</strong></td>
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<tr>
<td></td>
</tr>
<tr>
<td><strong>Solar flares</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Galactic cosmic rays</strong></td>
</tr>
</tbody>
</table>

• Single-event latch-up (SEL): Destructive fault; can affect the CMOS structure
• Single-event burnout (SEB): Destructive fault; affects power metal oxide semiconductor field-effect transistors (MOSFETs)
• Single-event gate rupture (SEGR): Fault that can damage the submicron structure
• Single hard error (SHE): Destructive fault in complex circuits

SET and SEU are the only transient faults. SEU is a failure that changes the value of a bit in a register or memory cell. A register with a logical value 1 is changed to a logical 0 after being affected or vice versa. SEU failures are also known as soft errors. Since the SET affects the functionality of transistors, creating an anomalous current, it can affect the final result of a logic operation. These transient faults can introduce a temporary error, so they will not affect future circuit operation.

3.3 CMOS Bulk and FDSOI Devices

The traditional industry standard, the MOSFET bulk technology, is facing problems with static power consumption and other second-order effects, in technology nodes below 130 nm. To try to handle these problems, one can explore new materials to replace silicon, such as hybrids like Ge-Si or gallium-arsenide, or try to replace the gate silicon oxide by other types of insulating materials to keep up with Moore’s law. Other devices are being developed in 3D, such as Fin-FETs, to keep increasing transistor density.

A set of structures was designed using TCAD simulation tools. Figure 3.3a shows a 32 nm predictive technology model (PTM) n-type MOSFET (NMOS) bulk transistor. This transistor has a p-type substrate doping of $4.12 \times 10^{18} \text{ cm}^{-3}$, a junction depth of 50 nm, a silicon oxide thickness $t_{\text{ox}}$ of 1.3 nm and a metal-gate work function $\Phi_{\text{M}}$ of 4.25 eV. Figure 3.3b presents a 28 nm FDSOI high-K NMOS transistor. This transistor is a p-type one, and it has a substrate doping of $1 \times 10^{14} \text{ cm}^{-3}$, a p-type channel doping of $1 \times 10^{15} \text{ cm}^{-3}$ with a thickness of 8.5 nm, an equivalent gate oxide thickness $t_{\text{EOX}}$ of 0.75 nm (SiO$_2$ thickness of 0.55 nm and HfO$_2$ thickness of 1.283 nm), a buried oxide (BOX) thickness of 20 nm, a p-type back plane (BP) doping of $2 \times 10^{18} \text{ cm}^{-3}$ with a thickness of 25 nm and a metal-gate work function $\Phi_{\text{M}}$ of 4.52 eV. Another 28 nm FDSOI transistor was also created with a 0.9 nm silicon oxide thickness, with the same characteristics and metal-gate work function as the 28 nm FDSOI high-K, to compare other geometry effects. Figure 3.4 shows a comparison between the $I_d$ and $V_g$ curves of these devices.
using the TCAD-created structures and the corresponding SPICE model card. For both devices, the width is $W_g = 300$ nm. Table 3.2 presents the characteristics of these devices under test.

### 3.4 Heavy-Ion Impact Simulation on Single Devices

In this case, the simulations were performed with the presented devices in the off state, such as shown in Figure 3.5a and b. Figure 3.5a presents a 32 nm bulk CMOS transistor setup, and Figure 3.5b shows a 28 nm FDSOI setup, where the BP terminal is grounded. In both cases, each device is biased with 1 V on the drain terminal. The device widths are $W_g = 100$ nm for both.

The heavy ion for the simulation was configured with $\text{LET} = 100 \text{MeV-cm}^2/\text{mg}$ (or 1.0447 pC/$\mu$m), a total track range $l = 300$ nm and a characteristic distance $w_t = 20$ nm. The total simulation time was $T_s = 100$ ps, and the heavy ion impacted at $t_i = 25$ ps (Calienes et al., 2015).

The simulated heavy ion impacted the raised terminals at six different angles $\theta$ (0°, 15°, 30°, 45°, 60° and 75°) and at five different locations $L_i$ (measured in nanometres from transistor spacers: 6, 12, 18, 24 and 30 nm) for each angle; that means 30 simulations. Figure 3.5c presents how the heavy-ion impact is performed using the distance $L_i$ and impact angle $\theta$. 

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**FIGURE 3.3**

Devices designed using TCAD tools. (a) 32 nm NMOS bulk. (b) 28 nm NMOS FDSOI.
Simulation of Single-Event Effects on FDSOI CMOS

The heavy-ion impacts on the drain and source terminals produce a transient current. To obtain the collected charge (CC) after the ion hit, it is necessary to integrate the transient current with respect to time for each $L_i$-$\theta$ pair (Calienes et al., 2015).

![Figure 3.4](image)

**TABLE 3.2**

<table>
<thead>
<tr>
<th>Electrical Characteristics of the Studied Devices</th>
</tr>
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<tbody>
<tr>
<td><strong>Parameter Name</strong></td>
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<tr>
<td>------------------------</td>
</tr>
<tr>
<td>Turn-on current ($I_{on}$)</td>
</tr>
<tr>
<td>Turn-off current ($I_{off}$)</td>
</tr>
<tr>
<td>Saturation threshold voltage ($V_{th,SAT}$)</td>
</tr>
<tr>
<td>Linear threshold voltage ($V_{th,LIN}$)</td>
</tr>
<tr>
<td>Drain-induced Barrier Lowering (DIBL)</td>
</tr>
<tr>
<td>Subthreshold slope (SS)</td>
</tr>
</tbody>
</table>

The heavy-ion impacts on the drain and source terminals produce a transient current. To obtain the collected charge (CC) after the ion hit, it is necessary to integrate the transient current with respect to time for each $L_i$-$\theta$ pair (Calienes et al., 2015).
3.4.1 Bulk Transistor of 32 nm

3.4.1.1 Heavy-Ion Impacts the Drain Terminal

The heavy ion with LET = 100 MeV-cm²/mg was impacted on the raised drain terminal of the 32 nm bulk transistor using the circuit configuration presented in Figure 3.5a, and the resulting CC is presented in Figure 3.6. The heavy ion produces a maximum CC of 32.29 fC when Li = 30 nm and θ = 30°. The minimum CC is 13.12 fC when Li = 6 nm and θ = 75°. The tendency in these conditions is for CC to decrease when the impact is near to the nitride spacer and the angle is increased.

![Simulation setup](image)

**FIGURE 3.5**
Simulation setup. (a) 32 nm bulk. (b) 28 nm FDSOI. (c) Heavy-ion impact setup. The “ø” symbol is part of circuits scheme in (a) and (b).

![Total CC results](image)

**FIGURE 3.6**
Total CC results of 100 MeV-cm²/mg heavy-ion impact on 32 nm bulk transistor drain terminal (Φ_M = 4.25 eV, W_s = 100 nm). (From Calienes et al., 2015.)
When the $L_i$ value is increased, CC tends to stay constant, with little charge variation; for example, with $\theta = 45^\circ$, CC is 27.27 fC for $L_i = 6$ nm, 30.80 fC for $L_i = 18$ nm and 31.27 fC for $L_i = 30$ nm. When $\theta = 15^\circ$, CC is even more constant.

When the impact angle $\theta$ is increased, the CC variation presents a 'sinusoidal' behaviour in all impact locations $L_i$; that is, CC is low at $\theta = 0^\circ$, higher at $\theta = 30^\circ$ and at $\theta = 75^\circ$ is lower than the charge at $\theta = 0^\circ$, as Figure 3.6 presents.

### 3.4.1.2 Heavy-Ion Impacts the Source Terminal

When the heavy ion impacted the source terminal of a 32 nm bulk transistor in the off state, the CC was less than the drain terminal impact case. Figure 3.7 shows this CC behaviour. The ion produces a maximum CC of 29.89 fC when $L_i = 12$ nm and $\theta = 60^\circ$, and the minimum CC is 2.31 fC when $L_i = 30$ nm and $\theta = 0^\circ$.

When $L_i$ is increased, the CC tends to decrease slowly, almost constantly; for example, when $\theta = 30^\circ$, for $L_i = 6$ nm the CC is 18.04 fC, for $L_i = 18$ nm it is 15.45 fC and for $L_i = 30$ nm it is 12.99 fC, as Figure 3.7 shows.

In the case of an increase in $\theta$, the CC increases up to $\theta = 60^\circ$, and then it declines slightly when $\theta > 60^\circ$; for example, when $L_i = 24$ nm, for $\theta = 0^\circ$ the

![FIGURE 3.7](image_url)

*Total CC results of 100 MeV-cm²/mg heavy-ion impact on 32 nm bulk transistor source terminal ($\Phi_M = 4.25$ eV, $W_g = 100$ nm).*
CC is 3.83 fC, for $\theta = 30^\circ$ it is 14.24 fC, for $\theta = 60^\circ$ it is 27.49 fC and for $\theta = 75^\circ$ it is 22.25 fC.

### 3.4.2 High-K FDSOI Transistor of 28 nm

#### 3.4.2.1 Heavy-Ion Impacts the Drain Terminal

In this case, the 100 MeV-cm$^2$/mg heavy ion impacted the 28 nm high-K FDSOI drain terminal. The simulation was conducted in the same way as the simulation of the bulk transistor. Figure 3.8 shows the CC as a function of $L_i$ and $\theta^\circ$. In this case, 5.13 fC is the maximum CC and it occurs when $L_i = 24$ nm and $\theta = 75^\circ$. The minimum CC is 0.45 fC when $L_i = 30$ nm and $\theta = 0^\circ$, a vertical impact far from the nitride spacer.

When $L_i$ is increased, the CC tends to decrease; for example, for $\theta = 45^\circ$, at $L_i = 6$ nm the charge is 2.78 fC, at $L_i = 18$ nm it is 2.23 fC and at $L_i = 30$ nm it is 1.31 fC. There are several exceptions at $\theta = 30^\circ$ and $\theta = 60^\circ$, but in general, the trend is met. If $\theta$ increases, the CC also increases. The minimum CC is when $\theta = 0^\circ$ and the maximum when $\theta = 75^\circ$, regardless of the impact location $L_i$.

#### 3.4.2.2 Heavy-Ion Impacts the Source Terminal

When the 100 MeV-cm$^2$/mg heavy-ion impacts the 28 nm high-K FDSOI source terminal, the maximum CC value is 4.46 fC at $L_i = 6$ nm and $\theta = 75^\circ$.

![Figure 3.8](image-url)

**FIGURE 3.8**

Total CC results of 100 MeV-cm$^2$/mg heavy-ion impact on 28 nm high-K FDSOI transistor drain terminal ($\Phi_m = 4.52$ eV, $W_g = 100$ nm).
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very close to the nitride spacer, and the minimum is 0.096 fC at $L_i = 30$ nm and $\theta = 0^\circ$, far from the nitride spacer. Figure 3.9 presents these CC tendencies in function of $L_i$ and $\theta$.

When $L_i$ increases, the CC tends to decrease slowly; for example, for $\theta = 30^\circ$, at $L_i = 6$ nm the CC is 0.38 fC, at $L_i = 18$ nm it is 0.24 fC and at $L_i = 30$ nm it is 0.15 fC. The exception is at $\theta = 75^\circ$, when the CC variation in function of $L_i$ is greater than at other impact angles. When $\theta$ is increased, the CC tends to increase in all cases. Regardless of the $L_i$ value, the maximum CC occurs when $\theta = 75^\circ$, and the minimum when $\theta = 0^\circ$.

3.4.3 FDSOI Transistor of 28 nm

3.4.3.1 Heavy-Ion Impacts the Drain Terminal

The 100 MeV-cm$^2$/mg heavy-ion impact on the 28 nm FDSOI drain terminal was performed in the same way as in the previous simulations. Figure 3.10 presents the result of the TCAD simulation for this case. The maximum CC is 4.20 fC and occurs when $L_i = 12$ nm and $\theta = 75^\circ$, close to the drain nitride spacer. The minimum CC for this case is 0.41 fC at $L_i = 30$ nm and $\theta = 0^\circ$, vertical and far from the spacer.

When $L_i$ increases, the CC tends to decrease; for example, for $\theta = 60^\circ$, at $L_i = 6$ nm the CC is 3.69 fC, at $L_i = 18$ nm the charge is 3.50 fC and at

FIGURE 3.9
Total CC results of 100 MeV-cm$^2$/mg heavy-ion impact on 28 nm high-K FDSOI transistor source terminal ($\Phi_M = 4.52$ eV, $W_g = 100$ nm).
Li = 30 nm it is 2.42 fC. The exception is when the impact occurs with \( \theta = 75^\circ \). In this case, the charge increases slowly from 3.58 fC at \( L_i = 18 \) nm to 3.74 fC at \( L_i = 30 \) nm. When the angle \( \theta \) increases, the CC also increases in all cases. The minimum CC values occur at \( \theta = 0^\circ \) and the maximum values occur when \( \theta = 75^\circ \), regardless of the impact location \( L_i \).

### 3.4.3.2 Heavy-Ion Impacts the Source Terminal

For the 28 nm FDSOI source terminal impact case, the maximum CC is 4.10 fC when \( L_i = 6 \) nm and \( \theta = 75^\circ \), and the minimum charge is 0.0706 fC at \( L_i = 30 \) nm and \( \theta = 0^\circ \). The CC behavior in this case is similar to the one with a drain impact, but in this case the CC is much lower. These results are shown in Figure 3.11.

### 3.4.4 Conclusions Related to Heavy-Ion Impact Simulation on Single Devices in Different Technologies

The collected transient charge and drain current peak depend on the substrate bias, lightly doped drain (LDD) geometry, silicon volume in the body/channel region, gate equivalent oxide thickness and polymeric metal-gate materials (Calienes et al., 2015). The generated charge due to an ion impact is collected by recombination, drift and diffusion processes. The
Simulation of Single-Event Effects on FDSOI CMOS

Transient peak current depends directly on the drift current component and substrate bias.

The quantity of CC is directly proportional to the silicon volume, and it also depends on the doping of the body (Calienes et al., 2015). In the ultrathin body and box (UTBB) FDSOI case, the silicon body thickness is less than the channel length and limited by the BOX. The recombination is lower than in the bulk transistor case, because the FDSOI silicon body is much thinner than in the bulk one. In the worst case, the CC in the FDSOI simulated transistors is smaller by a factor of approximately 7.68 than the worst-case CC in a bulk transistor. The electron density in the device is a measure of how the heavy-ion impact affects a device. Figures 3.12 through 3.14 show the variation over time of the electron density for each simulated device in the worst CC cases when a 100 MeV-cm²/mg heavy-ion impacts the drain terminal.

The most sensitive device area is the reverse-biased drain and source n-p junction (Messenger, 1982). In a bulk device, the maximum CC occurs when $L_t = 30$ nm and $\theta = 30^\circ$, when the ion track funnels through the LDD around the drain region, as shown in Figure 3.15a. A similar phenomenon occurs with a FDSOI device when $L_t = 12$ nm and $\theta = 75^\circ$, as in Figure 3.15b. In the high-K FDSOI case, this maximum CC occurs when $L_t = 24$ nm and $\theta = 75^\circ$. The CC difference between FDSOI and high-K FDSOI is small: 0.93 fC. In all cases, the ion funnels through the LDD and produces a maximum CC. Also,
FIGURE 3.12
Electron density over time in 32 nm bulk transistor when $L_i = 30$ nm and $\theta = 30^\circ$ ($\Phi_M = 4.25$ eV, $W_g = 100$ nm).

FIGURE 3.13
Electron density over time in 28 nm FDSOI transistor when $L_i = 12$ nm and $\theta = 75^\circ$ ($\Phi_M = 4.52$ eV, $W_g = 100$ nm).

FIGURE 3.14
Electron density over time in 28 nm FDSOI high-K transistor when $L_i = 24$ nm and $\theta = 75^\circ$ ($\Phi_M = 4.52$ eV, $W_g = 100$ nm).
the LDD doping in the bulk transistor is $-8 \times 10^{17} \text{cm}^{-3}$ and the LDD doping in both FDSOI transistors is approximately $-2 \times 10^{14} \text{cm}^{-3}$. The silicon doping in the body also has influence on the CC.

Simulations were also performed using different metal-gate work function $\Phi_M$ values in all transistors. Also, in the FDSOI cases, simulations were performed using devices with different gate equivalent oxide thickness $t_{EOX}$. The materials of the polymeric metal gate of the devices and the gate oxide thickness have influence on CC. The CC is formed by mobile charges generated when the heavy-ion funnels through the device, and the charge of the depletion zone $Q_d$. The charge $Q_d$ depends on the $\Phi_M$ and gate oxide capacitance $C_{ox} = \varepsilon_{EOX}/t_{EOX}$:

$$Q_d \sim C_{ox}(V_{th} - \Phi_M + \Phi_S + q(N_{ tox}/C_{ox}) - 2\phi_F)$$  (3.7)

where $\Phi_S$ is the body/channel semiconductor work function, $q = 1.602 \times 10^{-19} \text{C}$ is the electron charge, $N_{ tox}$ is the total oxide charge surface density and $\phi_F$ is the silicon Fermi potential. So, increasing $\Phi_M$ and $t_{EOX}$ decreases $Q_d$, and also decreases the total SET CCs (Calienes et al., 2015). If $t_{EOX}$ decreases, the device is predisposed to produce more CC due to a heavy-ion impact. The CC can be modelled as the sum of $Q_d$ and the mobile charges produced by the heavy-ion impact. Figure 3.16 presents a comparison between two 28 nm FDSOI transistors ($t_{ox} = 0.9 \text{ nm}$) with different $\Phi_M$: 4.25 and 4.52 eV (these data are used to obtain the data of Figure 3.10). The heavy ion has the same LET = 100 MeV-cm$^2$/mg and characteristics as in the previous simulations. The simulated impacts occur in two $L_i$ locations: 12 and 30 nm. Therefore, the
Semiconductor Devices in Harsh Conditions

transistor with $\Phi_M = 4.25$ eV collects more charge due to a heavy-ion impact than the $\Phi_M = 4.52$ eV one in a linear proportional relation, almost as predicted in Equation 3.7. This relation is no longer valid when the ion funnels through the drain, the LDD region and the body/channel at the same time. Figure 3.16 shows what happens in this case, when $\theta = 60^\circ$ and $L_i = 12$ nm: the CC in the $\Phi_M = 4.52$ eV case is greater than when $\Phi_M = 4.25$ eV.

The drain terminal is the most sensitive area in these devices, because in all cases, the heavy-ion impact on this terminal produces more CC than the impact on the source terminal. In this case, $V_{ds} = V_{db} = 1$ V is the voltage at the drain terminal and $V_{sb} = 0$ V is the voltage between the source and substrate terminals. In this case, the drain-body n-p junction is reverse biased ($V_{db} = 1$ V and the quasi-Fermi levels of the drain and body are different) and there is a large depletion region with a lot of depletion charge. In the source-body n-p junction case, the depletion region is thin due to the very low-voltage difference (in this case, $V_{sb} = 0$ V and the quasi-Fermi levels are almost the same). These depletion charges increase the total CC when the ion funnels through the device. In the bulk transistor, it is possible to have almost the same CC if the ion impacts both terminals with an angle $\theta > 45^\circ$, because there is the possibility to funnel into the LDD region from both the drain and source impact locations. In the bulk transistor, the channel region has a relativity high doping, and this increases the final SET CC. For the FDSOI devices, the low-doped channel region has a low charge contribution.
to CC after a heavy-ion impact. This fact, combined with the thin body/channel region and the bigger BOX region below the body/channel in the FDSOI transistor, would necessitate a very sharp angle (θ > 70°) for the ion to funnel through the LDD region and to obtain almost the same CC as having a heavy-ion impact on the source or drain terminals.

The BP and BOX in the FDSOI devices have advantages in a radiation environment. When the heavy-ion funnels through the device, the charges do not return to the channel, because the BOX isolates the charges, avoiding a contribution to the drain current. The grounded BP discharges the transistor substrate slowly (Calienes et al., 2015).

### 3.5 Heavy-Ion Impact Simulation on 6T Static RAM Cells

In order to simulate the effect of a heavy-ion impact on a six-transistor SRAM (6T SRAM) in these three devices, with the goal of comparing the radiation effects, it is necessary to create and set up the circuits for the test. The objective is to see what happens with the data stored in the cell and what is the minimum particle LET and CC to produce an SEU. The simulated memory cell schematic is shown in Figure 3.17 (Calienes et al., 2014). The cell is in retention mode with a supply voltage of 1 V, the word line (WL) is at 0 V and the bit lines (BL and BL') have 0 A current supply sources, to simulate high impedance. In this case, the TCAD simulation was performed in mixed mode; that is, five transistors were described using a SPICE model card and the impacted transistor was described at the device level. Tables 3.3 and 3.4 present the dimensions of each transistor in the three test circuits. The mnl transistor is the one suffering a heavy-ion impact in the drain terminal in the

![FIGURE 3.17](image_url)

Mixed-mode 6T SRAM cell. (From Calienes, W., et al., Impact of SEU on bulk and FDSOI CMOS SRAM, presented at Proceedings of 10th Workshop of the Thematic Network on Silicon-on-Insulator Technology, Devices and Circuits, Tarragona, Spain, January 29, 2014.)
worst-case CC for each device type. Transistors mnl and mnr have a bigger area than the other ones in this circuit. To simulate a logical 1 in the cell, the mnl drain (the OUTL node) is initialised at 1 V, while the mnr drain (the OUTR node) is initialised at 0 V. The BPs of the 28 nm FDSOI and 28 nm high-K FDSOI cells are tied to ground.

The total simulation time in all cases is $T_s = 1$ ns, and the heavy-ion impact occurs at $t_i = 0.490$ ns. The LET is variable. The $L_i$ and $\theta$ values are chosen from the previous device simulations to obtain the maximum CC.

### 3.5.1 Simulation Results of 32 nm Bulk 6T SRAM

Heavy ions with 1–10 MeV-cm$^2$/mg LETs were used to strike the drain terminal at $L_i = 30$ nm and $\theta = 30^\circ$ (the most disruptive condition for heavy-ion impact when the transistor is off state). Figure 3.18 shows the behaviour of the CC in the transistor mnl with different LETs. In these simulations, the minimum LET to flip the memory cell is 5 MeV-cm$^2$/mg, and it produced 1.91 fC of CC, but the minimum CC to flip the cell (the ‘critical charge’) for this circuit was $C_{ch} = 1.76$ fC. Using this $C_{ch}$ (Figure 3.18), the minimum estimated LET to flip the memory cell is approximately 4.75 MeV-cm$^2$/mg. The grey area in Figure 3.18 is the critical area where the memory cell has a bit flip.
3.5.2 Simulation Results of 28 nm FDSOI 6T SRAM

In this case, heavy ions with 60–70 MeV-cm²/mg LETs were used to impact the mnl transistor drain terminal at $L_i = 12$ nm and $\theta = 75^\circ$ (the worst case for this device in previous simulations). Figure 3.19 presents the results of the simulations for this memory cell. The grey area represents the critical area for the circuit. In the simulations, the cell flipped with LET = 64 MeV-cm²/mg and produced 2.03 fC of CC, but the $C_{ch}$ in this case was 1.78 fC when LET = 70 MeV-cm²/mg. The estimated LET to produce the $C_{ch}$ was approximately 63.6 MeV-cm²/mg, but it is possible to improve this result with more simulations using LET up to 90 MeV-cm²/mg. Figure 3.20 presents the voltage variation in the OUTL and OUTR nodes when a 64 MeV-cm²/mg heavy-ion impacts the mnl transistor drain terminal at $L_i = 12$ nm and $\theta = 75^\circ$.

3.5.3 Simulation Results of 28 nm FDSOI High-K 6T SRAM

In this simulation, the heavy-ion impacts on the mnl transistor were performed using 45–55 MeV-cm²/mg LETs. The drain terminal was hit at $L_i = 24$ nm and $\theta = 75^\circ$. Figure 3.21 shows the simulation results. The critical area for the circuit is shaded in grey. The minimum LET when the memory cell flipped was 50 MeV-cm²/mg, and it produced a CC of 1.89 fC. The critical charge is approximately $C_{ch} = 1.80$ fC when LET = 55 MeV-cm²/mg. LET = 49.7 MeV-cm²/mg is the minimum estimated LET to generate this approximate $C_{ch}$. 

![Figure 3.18](image-url)  
**FIGURE 3.18**  
CC vs. LET characteristics of 32 nm bulk 6T SRAM cell ($L_i = 30$ nm, $\theta = 30^\circ$). The grey area is the critical area when the cell flips.
3.5.4 Conclusions Related to the Heavy-Ion Impact Simulation on 6T Static RAM Cells

The flipping of a memory cell depends on the LET of the particle and the impact location in the transistor. In this case, to study the radiation effects,
only impacts on the large NMOS transistors \( m_{nl} \) and \( m_{nr} \) were considered, but this methodology is also valid in the case of p-type MOSFET (PMOS) transistors, when the memory cell is in retention mode. All measurements were done using the most critical locations and angles, that is, where the device is more susceptible to produce more CCs.

The 28 nm FDSOI memory cell is more resilient against heavy-ion impacts than the 32 nm bulk and 28 nm FDSOI high-K ones. The comparison of transient current pulses due to the heavy-ion impact, considering the worst cases for each cell, is shown in Figure 3.22. Table 3.5 shows the comparison among these cases. The 28 nm FDSOI cell is (in LET terms) 12.8 times more resilient than the 32 nm bulk cell, and 1.28 times more resilient than the 28 nm FDSOI high-K cell. In the three cases, the CC that flips a cell is almost the same, nearly 2 fC. The estimated critical charge \( C_{ch} \) is almost the same in the three cases: 1.78 fC. A \( C_{ch} \) ≥ 1.78 fC is needed to flip these memory cells. Therefore, almost the same \( C_{ch} \) needs to be generated to flip a cell in the three cases.

Figure 3.23 shows the electron density distribution as a function of time in the impacted transistor, in a 28 nm FDSOI high-K memory cell. A 50 MeV-cm\(^2\)/mg heavy-ion impacts the drain terminal at \( T_s = t_i = 0.5 \) ns. The ion produces CCs, and a transient current pulse is generated as shown in Figure 3.22, and the cell is flipped. The probability of the generation of a current pulse also depends on how the transistors are connected in the circuit and on the circuit layout. When the ion impacts the \( m_{nl} \) transistor drain terminal, the device is turned on briefly due to the charges produced by the impact; this voltage-level change in OUTL is sufficient to set in motion a positive feedback and flip the right-side inverter. This inverter changes its
output OUTR value to an effective ‘high level’ and turns on the mnl transistor (last picture of Figure 3.23).

The difference of the minimum LET to flip the 32 nm bulk memory cell and the 28 nm FDSOI memory cells can be explained by the difference in silicon volume of the affected device in each memory cell. The generated CC in the silicon is directly proportional to the LET times the distance travelled by the particle (Calienes et al., 2014).

The difference of minimum LETs between the 28 nm FDSOI memory cell and the 28 nm FDSOI high-K memory cell has another explanation. When the
equivalent oxide thickness $t_{\text{EOX}}$ is thinner, the $C_{\text{ox}}$ is greater, and the depleted charge $Q_d$ is directly proportional to $C_{\text{ox}}$, as shown in Equation 3.7. In the 28 nm FDSOI, $t_{\text{ox}} = 0.9$ nm, and this is the minimum silicon oxide thickness to avoid the gate tunnel effect. In the 28 nm FDSOI high-K, $t_{\text{ox}} = t_{\text{EOX}} = 0.75$ nm for the polymeric HfO$_2$-SiO$_2$ gate oxide. This silicon oxide thickness of the high-K cell avoids the gate tunnel effect because the total sum of the two oxide layers is 1.833 nm, which is greater than 0.9 nm. This is one of the reasons to choose high-K devices when the technology node is less than 90 nm.

3.6 Conclusions

The main conclusion is that a FDSOI CMOS transistor is more resilient to heavy-ion impacts than a bulk CMOS one. The volume of silicon in the active region and its doping are deciding characteristics in choosing this technology to cope with heavy-ion impacts. The BOX and BP regions avoid the back recombination in the channel region, depriving any drain current from the substrate charge. The CC with the FDSOI transistor was approximately 7.7 times less than with an identically sized bulk transistor in the worst case.

In all cases, the drain terminal was more sensitive to heavy-ion impacts than the source terminal. The CC depended on the depletion region thickness in the impacted terminal.

The SET CC in the tested devices did not depend on the impact angle. The CC depended on silicon volume in the body/channel, the body/channel doping, the gate equivalent oxide thickness, the polymeric metal-gate work function, the source/drain contact diffusion geometry and the LDD location.
The 28 nm FDSOI memory cells were more resilient than the 32 nm bulk ones. It can be concluded that for the three types of cells, the same amount of charge needs to be generated in the silicon to flip the SRAM cells. FDSOI also has the advantage of using a much thinner layer in the body/channel region.

The 28 nm FDSOI memory cell was more resilient than the 28 nm FDSOI high-K one. To avoid the tunnel effect in the gate insulator, it is necessary to choose the high-K cell. An equivalent oxide with a thin thickness predisposes a device to collect more charges when a heavy-ion impacts the device.

References


