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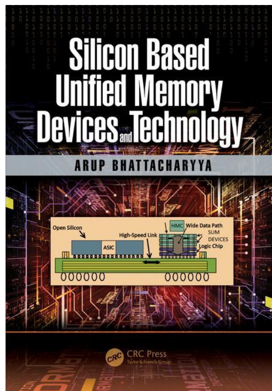

Silicon Based Unified Memory Devices and Technology

Arup Bhattacharyya

General Properties of Dielectrics and Interfaces for NVM Devices

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3 General Properties of Dielectrics and Interfaces for NVM Devices

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CHAPTER OUTLINE

Nonvolatile memory device performs as field effect transistor (FET) exhibiting multiple "stable" threshold states. These states are achieved by injecting charges (electrons and/or holes) from either the silicon substrate and/or the gate electrode, and by "permanently" holding the charges either into a floating storage medium or into a dielectric medium adjacent to the substrate to create appropriate threshold states. The dielectric media between the substrate and the gate and associated interfaces assume an essential and critical role in developing the characteristics of the nonvolatile memory device. This chapter will discuss the basic properties associated with dielectric films in general and related interface characteristics with silicon substrate and other dielectric, semiconductor, and metal films the context of FET gate stack structure. The selection and significance of various dielectric layers and interfaces in developing the characteristics of nonvolatile memories could be appreciated once the fundamental properties of materials and interfaces and roles played are understood.

3.0 THE NVM GATE STACK LAYERS AND INTERFACES

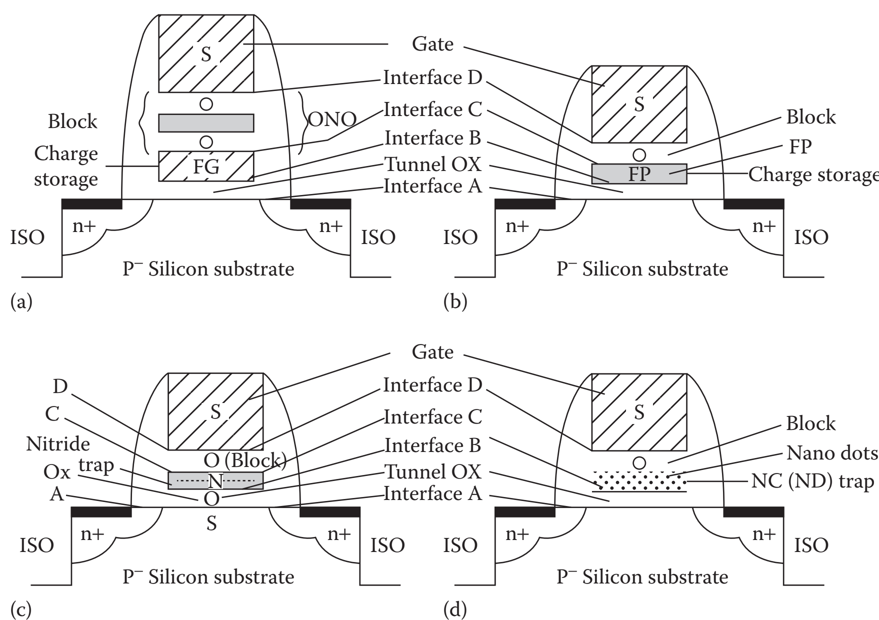

FIGURE 3.1 NVM device stack cross-sections: Dielectrics and charge storage layers and interfaces (A, B, C and D): (a) FG device, (b) FP device, (c) CT device, and (d) NC device.

3.1 ATTRIBUTES OF GATE STACKS FOR NVM DEVICES

The gate stack cross-sections of the conventional NVM-FET element for FG, FP (floating plate), CT, and NC (nanocrystal) devices are shown above in Figure 3.1a–d, respectively. The common elements are:

1. The silicon substrate.
2. *Interface A*: The silicon substrate with source and drain edges interfacing the tunnel dielectric layer defines interface A. This layer is a primary active layer for injection of electrons and holes from the silicon substrate.
3. *Tunnel insulator*: The tunnel dielectric above interface A had conventionally been SiO_2. The tunnel dielectric layer had been recently replaced by either SiON or high dielectric constant metal oxide or metal oxynitride, for example, HfO_2 or ZrO_2 or HfSiON or in some advanced devices, multiple very thin tunnel dielectric layers such as oxide/nitride/oxide (ONO). Advanced device tunneling layers employing higher dielectric constant metal-oxide films as mentioned above have been discussed in this book in Part II Chapter 12.
4. *Interface B*: This interface layer exists between the tunnel dielectric and the charge storage medium. In the conventional FG device, the polycrystalline silicon (doped or undoped) with associated grain edges interface the amorphous tunnel insulator. In the case of FP device, the interface could be an amorphous silicon-rich nitride (SRN) layer with high concentration of silicon nanocrystals at the interface. In the case of CT devices, the interface is typically a transitional oxide–nitride interface, both layers being amorphous. Finally, for the NC devices, the interface could either be similar to CT devices if the nanodots are embedded in nitride (as in SRN or nitride) or could be relatively uniform when the nanodots are embedded into deposited oxide.
5. *Charge storage layer*: The charge storage layer is deposited over the tunnel dielectric layer. For the FG device, this is the polysilicon layer. For the FP device, this is the injector SRN layer, which could be considerably thinner (<5–10 nm) compared to FG thickness, which could be >>10 nm. For the CT device, typical nitride thickness may be around 6–10 nm although thinner nitride layers may also be used for SONOS devices. For NC devices, the charge storage layer is similar in thickness comparable to SONOS nitride layer.
6. *Interface C*: This interface layer exists between the charge storage layer and the blocking dielectric layer. This interface is similar in characteristics to interface B.
7. *Charge blocking layer*: The charge blocking insulator layer is deposited over the charge storage layer. For the FG device, conventionally, with polysilicon control gate (CG), this layer is often called interpoly dielectric or IPD layer, being a single dielectric layer or multiple dielectric layers between the FG and the CG. For the FG device, this is typically an ONO structure with an equivalent effective oxide thickness (EOT) (equivalent oxide thickness, defined later on in the text) of 10 nm. For the FP device, this could be similar to the FG device but thinner. For the CT and NC devices, this could be oxide only with thickness around ~5 nm. For advanced device structures, charge blocking layer is currently often a single or multilayer high K dielectric film, for example, alumina or HfO_2 or ZrO_2 or HfSiON to reduce the stack EOT and thereby the writing and erasing voltage level requirements for the device.
8. *Interface D*: This interface layer exists between the blocking dielectric layer and the CG. Similar to the interface layer A, this layer is also a primary active layer for injection of electrons and holes from the CG.
9. *Control gate*: The CG could be either a heavily doped polysilicon layer (“S”) or Metal or Metal Silicide (“M”). In recent years with feature size scaling, the CG is increasingly being changed from polysilicon gate to metal gate and often typically changed from

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multigrain interface D associated with polysilicon grain to smoother interface D with metallic nitride such as titanium nitride (TiN) or tantalum nitride (TaN). Some popular SONOS devices are now called TANOS (TaN/alumina/nitride/oxide/silicon) device with associated change in blocking layer and gate material. The TANOS devices will be discussed in Part II Section 13.5.4, in this book.

The sidewalls of the gate insulator stack are isolated along the length and width of the FET channel by thicker oxide and associated interfaces. These regions are considered relatively passive and not taken into consideration from device characteristics point of view. However, as feature size is scaled, parasitic capacitive coupling with neighboring memory cells and associated disturb becomes important in device characteristics, which will be discussed in this book. Additionally, fringing fields due to edge effects associated with device isolation (shallow trench isolation, "STI," not shown, along the device width direction) also affect device characteristics when feature size is scaled. This will also be discussed in the later chapters of this book.

It should be noted, therefore, that all devices have at least four active interfaces and at least three dielectric layers and either metal or silicon gate. The characteristics of the interfaces, gate material, and the dielectric layers have profound impact on the various NVM device properties. This section will review the material properties of these layers and their significance on NVM device characteristics.

3.1.1 The Energy Band of the Gate Stack Layers

The gate stack layer of the NVM device with the associated dielectric layers and interfaces can be depicted in terms of the energy band diagram identifying the different elements in the stack design. As an example, the energy band diagram for the conventional floating-gate device is illustrated in Figure 3.2. On the left, is the silicon substrate with the energy band gap Eb = 1.1 eV. On the right, is the metal or silicon gate with the electronic work function (energy required to remove an electron from the gate to vacuum: WF; for silicon gate, WF = 4.1 eV) with reference to the vacuum. The tunnel dielectric oxide layer, the silicon floating gate charge storage layer, and the oxide-nitride-oxide (ONO) charge blocking layers are identified with their appropriate band gaps. The interfaces are identified with the shaded region. The potential energy barriers (U) or (Φ) [used interchangeably in this book] are identified as: the first suffix for electrons (e) and holes (h) and the second two-letter suffix relate to the function of the dielectric layer: "tu"

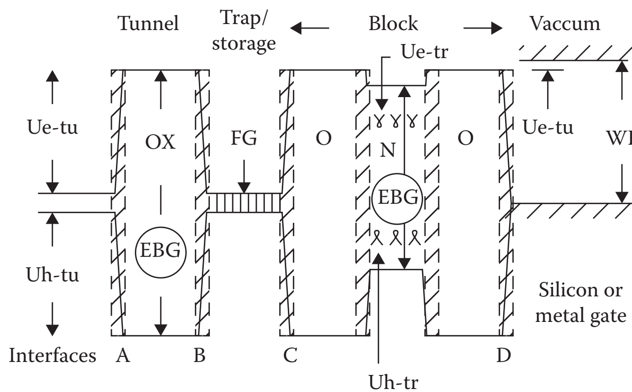

FIGURE 3.2 Energy band diagram for the FG stack: The band gap EBG for silicon, SiO_2, and Si_3N_4 are, respectively, 1.1, 9.0, and 5.1 eV; Ue−tu, and Uh−tu are respectively 3.2 and 4.7 eV, Ue′−tu for silicon gate is 4.3 eV and Ue−tr for nitride is 1.1 eV.

for tunneling, "tr" for trapping, and "bl" for blocking. Therefore, Ue–tu (or Φe–tu) implies the energy barrier for electron tunneling, Ue–tr (or Φe–tr) is the electron trap energy depth, and so on. The band diagrams are extremely useful means to recognize the energetics associated with the interface barriers impacting electrons and hole transport in metal/insulator/semiconductor structures. Band diagrams has been used extensively in this book to qualitatively explain various modes of electronic charge transport through NVM devices and consequently NVM device properties. It should be noted, however, that in many illustrations and especially with complex gate stack designs employing multilayered dielectric films, interface modulations of potentials (and associated energy) are ignored for simplicity.

3.2 GENERAL PROPERTIES OF THIN DIELECTRIC FILMS

Properties of thin dielectric films can be broadly categorized into three groups: (1) Physical, chemical, and thermal stability and associated reliability and breakdown strength; (2) Electronic properties such as dielectric constant, transport properties, and band gaps; and (3) Process-sensitive properties such as compositional uniformity or stoichiometry, scalability, interface properties such as fixed charge density, interface states density, and trap density. Selection of thin dielectric films has been a critical aspect of the evolution of microelectronics.

Since multiple layers of thin dielectric films are employed in the gate stacks of nonvolatile memories, commonly used thin dielectric films and future possibilities will also be discussed in this chapter addressing potential advantages and limitations of potential options.

The above discussion would be limited to amorphous thin dielectric films only, and to those dielectric films maintaining amorphous characteristics during the processing temperatures of 0°C–1000°C (typical of microelectronic device fabrication) without undergoing any structural transformations. Crystalline formations create defects along the grain boundaries and consequently exhibit higher leakage. Therefore, crystalline dielectric films are not suitable for microelectronics and nanoelectronics applications and will not be considered even if such dielectric films exhibit otherwise desirable dielectric characteristics.

3.2.1 Physical, Chemical, and Thermal Stability

Physical, chemical, and thermal stability of amorphous bulk dielectrics as well as thin films is dependent on purity, local, and long-range compositional uniformity, local and long-range bonding, electronic structure (position in periodic table of elements), and electron affinity. Most dielectric compounds exhibit either ionic or covalent bond characteristics, which determine their bond strength. A good indicator of the bond strength and related thermal stability associated with bulk or thin films of any dielectric is its melting point. The higher the melting point, the stronger is the bond strength.

Ionic bonds are established between metal cations and oxygen or silicates or halides to form stable metal oxides or silicates or halides. For oxides, metals exchange one, two, three, or four electrons (dependent on the energy states of the electrons in the outer orbitals, position in periodic table) with oxygen to form corresponding ionic bonds for crystalline dielectric establishing long-range order. In contrast for amorphous solid dielectrics, such bonding exists with short-range order only. Bond strengths in metal and semimetal (semiconductor) oxides are generally related to the electronic structure of the metal (or semimetal) and the number of electrons exchanged with oxygen to form stable inorganic compounds. For example, silicon (Si) and zirconium (Zr) with four electronic exchange form respective oxides of SiO_2 and ZrO_2 with high bond strength. Lanthanides (La, Pr, Sm, etc.) form corresponding oxides: La_2O_3, Pr_2O_3, Sm_2O_3, and so on possessing intermediate bond strength. Whereas metals such as Ba and Sr form BaO and SrO, respectively, with two electronic exchange exhibiting lower bond strength. Exceptions exist for metals such as aluminum, titanium, and tin.

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TABLE 3.1
Melting Point and Dielectric Strength of Common Dielectric Materials

	SiO_2	Si_3N_4	Al_2O_3	TiO_2	ZrO_2	HfO_2
Melting point: C	1710	1900	2015	1640	2710	2810
Dielectric strength/cm	>10	10	5–10[a]	low[a]	≥4[a]	≥6[a]

[a] Strongly process sensitive.

In case of Aluminum (AL) with three electron exchange forming Al_2O_3 results in bond strength as nearly as strong as SiO_2. Titanium (Ti) could exchange 3 or 4 electrons forming, respectively, Ti_2O_3 and TiO_2 exhibiting intermediate bond strengths. In contrast, Tin with four electronic exchange forming SnO_2 exhibits lower bond strength. However, it is generally expected that metals with similar electronic structure will exchange electrons with oxygen in a similar manner. Therefore, such exchanges will result in similar characteristics related to thermal and chemical stability as well as short-range order from thermodynamics and reaction kinetics.

Electronegativity (or electron affinity for dielectric) is also an important parameter, which relates to bond formations and stability of dielectrics. While large difference in electronegativity between oxygen and metal results in ionic bonding, elements with similar electronegativity form covalent dielectric. Silicon carbide (SiC) is a good example of covalent stable dielectric and has wide application in electronics. Electron affinity and band gap of dielectrics are related and will be discussed in the section on electronic properties.

Melting point and dielectric strength of some common dielectric materials are shown in Table 3.1.

Breakdown strength and reliability of thin dielectric films will be discussed later on in a separate section. Both breakdown strength and reliability depend on material stability but also on electronic properties and process sensitivity.

3.2.2 Electronic Properties

Key electronic properties of dielectric materials as well as dielectric films for nonvolatile memory applications are: (1) Band gap and electron affinity, (2) Charge holding capacity or dielectric constant, (3) Destructive breakdown strength, (4) Leakage or charge transport characteristics, (5) Reliability under electrical stress, and (6) Interface characteristics and stability with reference to silicon substrate and gate electrode metallurgy, plus interface characteristics between different insulators when multilayer insulators are involved. A significant parameter in nonvolatile devices that are related to the above list is “EOT,” and the second one is “scalability.” These are also discussed in the section below.

Band gap and electron affinity: Dielectric materials prevent charge movement within the material and have the capacity to hold charges at the meta–dielectric interface. This is related to the energy barrier between electrons and holes called band gap. The larger the band gap, the less conductive the dielectric material under voltage stress. Electron affinity is defined as the energy difference between dielectric conduction band and vacuum. It represents the energy required to remove an electron from the dielectric material. The higher the electron affinity, the more chemically reactive the dielectric material with other elements at the interface in electronic exchanges. The band gap and electron affinity are represented as Eb and Ue, respectively. Dielectric materials with large band gap and low electron affinity provide low leakage and high breakdown strength. Both silicon

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dioxide (SiO_2) and alumina (Al_2O_3) are characterized by such attributes and are widely used in electronics. Eb and Ue for SiO_2 and Al_2O_3 are, respectively, 9 eV and 0.9 eV for SiO_2 and 8.7 eV and 1.35 eV for Al_2O_3. Both insulators exhibit high breakdown strength: >10E6 V/cm and low leakage. In contrast, insulator such as TiO_2 has a low band gap of Eb = 3.5 eV and large electron affinity of Ue = 4.1 eV. Consequently, TiO_2 films have limited applicability due to high leakage in spite of its high charge holding capacity (dielectric constant of 80).

Charge holding capacity or dielectric constant: Dielectric materials are used to hold charges as capacitors. Capacitor charge density is expressed in terms of capacitance per square micrometer in the form of $fF/\mu m^2$. One way to characterize the charge holding capacity of a dielectric is its dielectric constant (K), which is the ratio of its permittivity to that of vacuum characterizing the dielectric constant of vacuum as K = 1. The higher the dielectric constant, more is the capacity to hold charge. Thin SiO_2 films have a K value equal to 3.9, while a thin Al_2O_3 film could have a K value nearly equal to 9. Therefore, the same thickness of Al_2O_3 can hold ~2.3 times electronic charge when compared to the same thickness of SiO_2 film. For reasons to be discussed later on, SiO_2 films had been the reference dielectric films for the microelectronics industry. For technology scaling purposes, it is convenient to express other dielectric films in reference of "Equivalent SiO_2 oxide thickness" or "EOT." EOT is the ratio of dielectric constant of another dielectric film when compared to that of SiO_2 film. For the same geometry, EOT implies the scalability factor when SiO_2 film is replaced by a different dielectric film to achieve the same value of capacitance. Therefore, EOT of Al_2O_3 would be nearly 3.9/9 = 0.43× of those of SiO_2.

Dielectric breakdown or dielectric strength: When sufficient electrical field is applied across a dielectric capacitor, electrons and holes get injected into the body of the dielectric and get transported across the dielectric exhibiting current flow. With increasing field, current flow increases. Eventually, at a certain critical field, permanent conductive path (or paths) is established and the dielectric breaks down and loses charge holding capacity. The field at which such destructive breakdown takes place is called the breakdown strength of the dielectric and is typically expressed in mega volts/cm or MV/cm. In general, the breakdown strength of a bulk dielectric is intimately related to the band gap and bond strength and chemistry of the dielectric. However, in thin dielectric films, the breakdown strength is influenced by local defects, compositional nonhomogeneity, surface irregularities, and process parameters. For ultrathin dielectric films, surfaces and interfaces play increasingly important role in determining the breakdown strength. Dielectric reliability is connected to the breakdown strength. The higher the breakdown strength, more reliable the dielectric is expected to be. Well processed and relatively defect-free SiO_2 films exhibit breakdown strength greater than 10 MV/cm, while ultrathin SiO_2 films show breakdown strength significantly higher. Table 3.2 shows schematic representation of electronic affinity, band gaps, and dielectric constant of common metal-oxide dielectric films against those of silicon and Ge substrates.

Charge confinement and charge transport characteristics: Amorphous dielectric exhibits the capacity to hold charges in the body of the dielectric, what are known as defect centers or traps. When sufficient potential is applied across the dielectric, both the electrodes as well as the charge centers could be active in providing charges to flow in response to the potential imposed. These phenomena known as charge trapping and charge detrapping and field plus temperature-induced charge flow are critical to the characteristics of FETs, and especially to the attributes of nonvolatile memory devices. These will be elaborated below.

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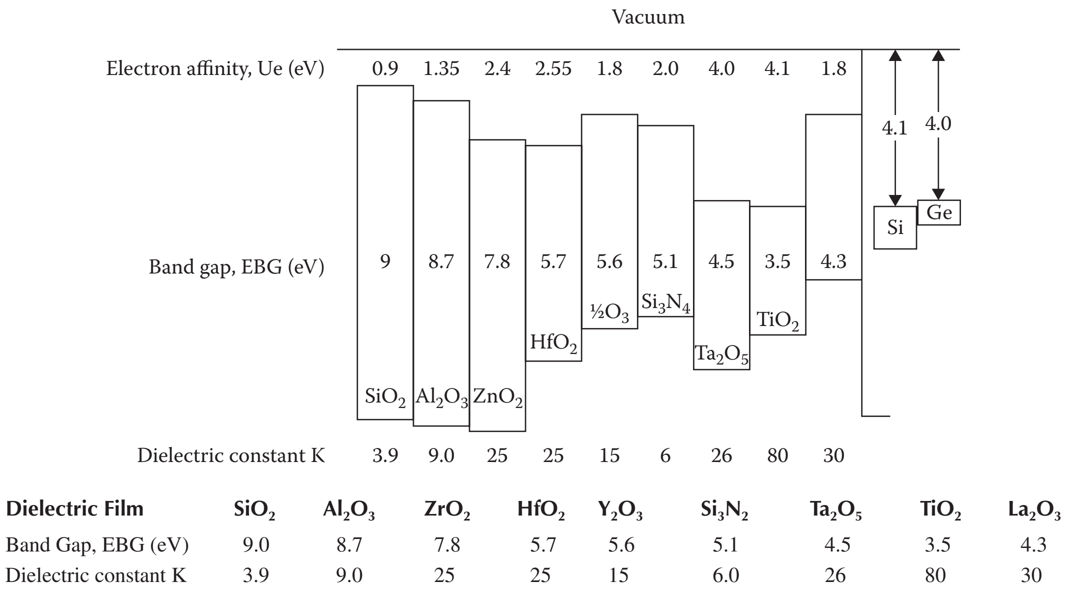
TABLE 3.2
Schematic Representation of Electron Affinity (Ue), Band Gap (Eb), and Dielectric Constant (K) of Common Metal Oxide Films against Ue of Silicon and Germanium



Dielectric Film	SiO_2	Al_2O_3	ZrO_2	HfO_2	Y_2O_3	Si_3N_2	Ta_2O_5	TiO_2	La_2O_3
Band Gap, EBG (eV)	9.0	8.7	7.8	5.7	5.6	5.1	4.5	3.5	4.3
Dielectric constant K	3.9	9.0	25	25	15	6.0	26	80	30

3.2.3 Bulk and Interface Defects and Charge Trapping

Amorphous dielectrics contain varying degrees of compositional nonhomogeneity within the bulk of the material. Such nonhomogeneity manifests at the molecular dimensions into defect centers often called traps. Such traps create local potential well providing local confinement of charges. Traps could be positively charged (with trapped holes), or negatively charged (with trapped electrons), or neutral. Additionally, fluctuations in nuclear potentials give rise to fixed charge centers either positive or negative within the bulk dielectric as well as at the interfaces. Furthermore, energy states are generated within the forbidden band gap due to the presence of impurities and variation in local chemistry. In planar thin dielectric films, surfaces provide broken chemical bonding as well as chemical nonuniformity. In a field effect transistor structure (FET device), a thin dielectric film (e.g., SiO_2) is in contact with the silicon substrate. In such a case, the interface can generate fixed charge centers as well as interface energy states, which adversely affect device properties. In a multi-, dielectric gate insulator stack, the interface created by the two dielectric layers of different chemical composition provides discontinuity in chemical bonding as well as thermomechanical stresses. This may result in increased defect density at the interface and associated trap density and interface states. Similarly, when a dielectric film interfaces a metal gate or a polysilicon gate (doped or undoped or a floating gate, examples being FET or FLASH devices, respectively), the interfaces created are chemically, thermally, and mechanically nonideal. The resulting interfaces give rise to interface defects, traps, fixed charges, and interface energy states. As devices get scaled in dimensions, interfaces become increasingly important in influencing different device characteristics including charge transport.

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3.2.4 Charge Transport

In thicker dielectric films, charge carriers, electrons, and holes exist in bulk traps. In thick or thin films, such carriers could also be provided by the electrodes interfacing the dielectric film. For example, in metal–insulator–silicon (MIS) capacitors or devices, charge carrier sources could be metal at one end and silicon at the other end. When a voltage stress is applied across the insulator (dielectric) film, charge carriers could be provided either from the bulk dielectric or from the electrodes, that is, metal or silicon or both. Depending on the polarity of the stress and the magnitude, electrons will flow toward the positive terminal (anode), while holes will flow toward the negative (cathode) terminal. This results in leakage and current conductivity in the dielectric reducing its capacity to store charge. When the charge source is bulk dominated, current flow is bulk controlled reflecting the bulk characteristics of the dielectric film. Whereas when the current source is electrode controlled, either metal or silicon, the current transport is electrode controlled and reflects the interface energy states of the metal (work function) or silicon (band energy or interface energy levels).

Multiple examples of carrier transport exist in dielectric films. Even in a particular dielectric film, transport mechanisms may change depending on the stress level, processing history, chemistry, and so on, and several mechanisms may be operative. The most significant bulk-controlled mechanism is called the Poole–Frankel mechanism, which involves transport of trapped charges released due to thermal excitation. Such mechanism is field enhanced and sensitive to temperature. Another variation of above mechanism prevalent in dielectrics with shallow traps involves hopping by thermal excitation from one shallow trap to another with strong temperature dependence. Another variation which has weak temperature dependence and is present in dielectrics with relatively shallow trap is called resonance tunneling or trap-assisted direct tunneling. All the above mechanisms are bulk controlled.

In contrast to the above mechanism, a significant electrode-controlled mechanism based on quantum mechanical tunneling of charge transport is called the Fowler–Nordheim (FN) tunneling. For thicker dielectric films with carrier sources being electrode controlled, this transport mechanism is prevalent with strong field dependence and weak temperature dependence. For very thin films, direct quantum mechanical tunneling transport of carriers takes place, which has no temperature dependence but is strongly dependent on voltage and dielectric film thickness. A variation of the FN tunneling is called enhanced FN tunneling where transport of carrier is enhanced by local high-field effects at the interface.

Carrier transport mechanisms determine how conductivity of any dielectric film is sensitive to field across the dielectric film and temperature. Since these mechanisms are of considerable interest in nonvolatile memory devices, all above mechanisms will be discussed in greater detail in a separate section on Dielectric Conductivity.

3.2.5 Figure of Merit for Selected Metal-Oxide Dielectric Films

Using oxide (SiO_2) as a reference dielectric, a commonly used figure of merit is often employed to compare potentially applicable metal-oxide dielectric films as a replacement for oxide in FET device and memory applications [1]. This figure of merit combines the charge holding capacity (dielectric constant) with a permissible dielectric leakage level and expresses in terms of EOT providing a useful parameter for device application. Assuming the SiO_2 film reference limit of thickness 3.5 nm and leakage level ≤1E-3 A/cm^2 at 1.25 V (field of ~3.6 MV/cm), charge holding capacity of other dielectric films is compared for the same leakage level. This is shown in Table 3.3 for selected metal-oxide dielectric films of interest. The figure of merit demonstrates

TABLE 3.3
Single Metal Oxide Figure of Merit [1]

	SiO_2	Al_2O_3	ZrO_2	HfO_2	Ta_2O_5	TiO_2
Band gap: EBG, eV	9.0	8.7	7.8	5.7	4.5	3.5
EOT: nm	3.5	1.8	1.7	1.5	3.75	2.8
Thickness: [a] nm	3.5	5.5	8.5	13.6	25.0	58.0
Capacitance: [a] fF/μ²	10	~20	~20	~17	~9	~12.5
Figure of merit	1	2	2	1.7	0.9	1.25

[a] Ref: SiO_2: Leakage limit: 1E-3A/cm² at 1.25 V.

that higher K metal oxides such as TiO_2 ($K = 80$) and Ta_2O_5 ($K = 26$) may not be appropriate replacement for SiO_2 due to considerably higher leakage. On the other hand, alumina and zirconia films are similar in figure of merits (2× of SiO_2) and worthy of consideration even though the latter has the 2.5× enhancement in K value. HfO_2 film also exhibits enhanced figure of merit compared to SiO_2.

3.2.5.1 Metal Work Function and Electron Affinity

For MIS types of devices (here metal [M] also includes heavily doped silicon electrode), work function (Wf) for metal electrode interfacing the dielectric (I) is an important parameter. While work function is the energy required to remove a "free electron" from the metal electrode to vacuum, the electron affinity, Ue for the dielectric (I) is the corresponding energy required to remove an electron from the conduction band of the dielectric to the vacuum. When the difference between work function and electron affinity (Wf-Ue) is large, charge injection from the metal electrode to the insulator is minimized, thereby minimizing both charge trapping and charge transport. Similarly, larger band gap insulator (I) at the silicon substrate, (S), interface ensures electron or hole injection into the insulator to minimize charge trapping and transport at the substrate side. Figure 3.3 shows metal work functions values in a schematic representation. Corresponding values for silicon and germanium are, respectively, 4.1 eV and 4.0 eV.

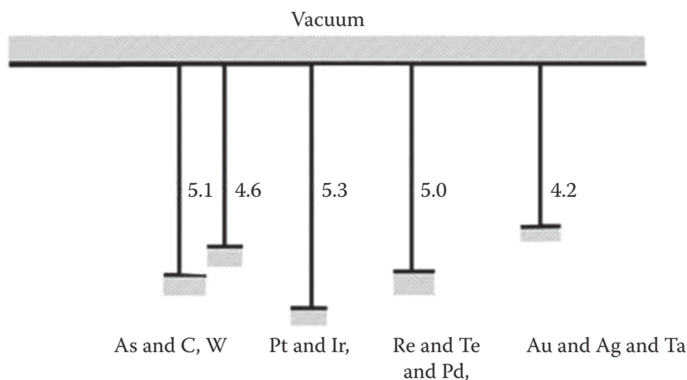

FIGURE 3.3 Work functions of As, C, and metals: Pt/Ir (5.3 eV); Re/Te/Pd (5.0 eV); and Au/Ag/Ta (4.2 eV).

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3.3 INTERFACES, ELECTRODE COMPATIBILITY, AND PROCESS SENSITIVITY

We have defined various interfaces for the NVM devices at the beginning of the section (Figure 3.1) and discussed some aspects of the metal–insulator and insulator–silicon interfaces earlier. For multiple dielectric layers, there are additional interfaces created between the dielectric layers as well as between each dielectric and silicon and other interfacing electrode. Since interfaces involve transition of one material chemistry to another, the processing goal is to minimize defect creation at the interfaces, which gives rise to traps, interface states, fixed charges, and so on as mentioned earlier. Interfaces are expected to be free of contaminants, clean, and discrete. Interface properties to consider are of physical, chemical, and electronic in nature. Physical compatibility implies materials selection to reduce thermal mismatch and stresses at the interface and to ensure adhesion and stability during processing and post processing conditions. Chemical compatibility involves bond stability during processing and post processing variables such as temperature, pressure, and chemical environments. Electronic compatibility involves reproducibility and stability of energy states with reference to electrons and holes.

Microelectronics involves extensive applications of MIM (metal–insulator–metal) and MIS (metal–insulator–silicon) elements as passive and active device elements. Therefore, compatibility with electrode material is also extremely important in achieving desirable characteristics. Electrode compatibility involves material selection to simultaneously achieve, (a) large work function difference to minimize charge injection from the electrode to the insulator, (b) reduce inter facial stress and thermal mismatch, (c) physical/chemical/mechanical integrity during processing and post processing conditions of temperature and ambient, and (d) process reproducibility and ease of fabrication of dielectric and electrode materials. From process integration point of view, additional requirements include selective patterning of deposition and etching, thickness uniformity, and control.

Process sensitivity relates to process techniques and variables in process parameters impacting the properties of the dielectric films. It has been well known that dielectric thin-film properties (bulk as well as surface) are process sensitive. Properties impacted include physical properties such as adhesion, stresses, thickness uniformity, and refractive index, chemical properties such as purity, compositional uniformity, chemical bonding, and etch rate, electronic properties such as band gap, dielectric constant, leakage, electron affinity, trap density, and fixed charge density. There are a wide variety of processing techniques to deposit dielectric thin films. These include thermal deposition and oxidation, chemical vapor deposition (CVD, MOCVD, and LPCVD), plasma deposition and sputtering, and atomic layer deposition (ALD). Processing parameters and variables involve: chemical species, temperature, pressure, ambient, partial pressure of chemical constituents, and deposition rate. These will be discussed in greater detail with reference to selected specific dielectric films widely used in nonvolatile memory technology.

3.4 GATE MATERIAL FOR NVM DEVICES

In general, gate materials employed for NVM devices are required to be CMOS technology compatible. Gate materials employed in NVM device elements are rarely different from PFET and NFET CMOS gates due to technology scalability considerations and process integration requirements. Typically, CMOS technology had employed either N-doped or P-doped polysilicon gates in the past, which are being progressively changed to metal gates for FET device scaling requirements. In Part II of this book, we have discussed in detail the integration schemes and compatibility requirements for the scaled NVM technology with those of general scaled CMOS technology. Aside from the polysilicon gates, the most common metal gates employed in NVM devices are metal nitrides, namely, TiN and tantalum nitride (TaN). Metal nitride films are compatible to general CMOS technology and provide large work function barriers to prevent undesirable charge injection from the

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metal gate during writing or erasing. These layers are deposited on top of the blocking dielectric layers followed by the desired thicker metal interconnect levels (e.g., tungsten metallurgy) for the CMOS technology.

3.5 DIELECTRIC CONDUCTIVITY MECHANISMS

3.5.1 Bulk-Controlled Poole-Frenfel Mechanism

This mechanism of conductivity is also known as Internal Schottky Mechanism and often referred to as mechanism of transport due to field enhanced thermal excitation of trapped carriers. Conductivity of a dielectric film exhibiting Poole–Frenkel mechanism is given by:

$$J/E = C \exp[-q\{\Phi e\text{–}tr - (qE/PI€_0 K_d).5\}/kT\}$$

where

J/E is the conductivity, J being the current density and E being the electric field defined by externally applied, voltage divided by the thickness of the dielectric film that is, V/d
C is a characteristic material constant
q is the electronic charge
Φe−tr is the trap energy depth from the conduction band edge
PI is the mathematical constant (value 3.14)
$€_0$ is the permittivity of the free space
K_d is the dielectric constant of the dielectric film
k is the Boltzmann constant (value 1.38046 E-16)
T is the body temperature of the dielectric film

Many common dielectric films such as silicon nitride (Si_3N_4), wide ranges of silicon oxynitrides (SixOyNz), and alumina (Al_2O_3) exhibit Poole–Frenkel Transport over a major range of voltage stress. As stated earlier, the conductivity is sensitive to temperature and increases with increasing temperature.

Dielectric film parameters such as the trap energy depth Φe–tr and dielectric constant K_d also strongly influence the conductivity of the dielectric film.

Two other bulk-controlled mechanisms are observed in thin dielectric films. The first one is strongly temperature sensitive and is present in dielectric films associated with very shallow traps. This mechanism is called "Hopping" and involves hopping of charge carriers from one shallow trap to another shallow trap due to thermal excitation. The second one exhibits weaker temperature dependence and is called "trap-assisted direct tunneling" or "Resonant Tunneling." This mechanism is displayed at low field and at low current ranges with current density being exponentially proportional to the voltage. Silicon-rich oxides (SROs) and SRNs as well as others exhibit such characteristics at lower field and at room temperature. Schematic representations of all three bulk-controlled mechanisms are shown in Figure 3.4a–c, respectively, for Poole–Frenkel, multiple trap hopping, and trap-assisted direct tunneling.

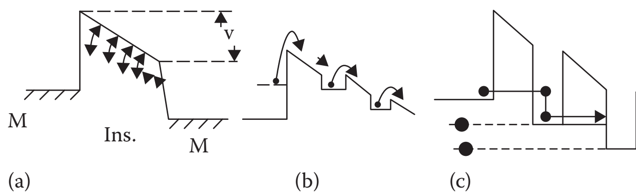

FIGURE 3.4 Bulk-controlled mechanisms: (a) Poole–Frenkel (Temperature sensitive), (b) Trap Hopping (strong temperature sensitive), and (c) Trap-assisted direct tunneling (weak temperature sensitive).

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3.5.2 Electrode-Controlled Quantum Mechanical Tunneling Mechanisms

There are generally three modes of quantum mechanical tunneling, which are all electrode controlled whereby the carriers (electrons or holes) are supplied by the electrode (silicon or metal). These are (a) Direct Tunneling or modified Fowler–Nordheim tunneling; (b) Fowler–Nordheim tunneling; and (c) Enhanced Fowler–Nordheim tunneling.

3.5.3 Direct Tunneling and/or Modified Fowler–Nordheim Tunneling

In this mode of transport, electrons or holes incident at the electrode–dielectric interface facing a potential barrier of trapezoidal type as shown in Figure 3.5a and b and exhibiting a finite probability of movement across the potential barrier, which is exponentially dependent directly on the voltage and inversely on the thickness of the dielectric film or films (case b), when the external voltage is less than the potential barrier. The transport of electrons or holes by this mechanism is characterized by the following equation:

$$Jt \sim De.Pt$$

Where Jt is the tunnel current density and is equal to: I/A, I being the current, and A is the injecting electrode surface area; De is the electron density at the barrier interface where the barrier potential is Φb and Pt is the tunneling probability. The tunneling probability Pt is given by:

$$Pt = \exp(-\Phi b^{0.5}.d)$$

Where d is the dielectric thickness. When two thin dielectric films are involved as could be illustrated for an MNOS device consisting of ultrathin layers of both oxide and nitride as in the case of Figure 3.5b, the transport mode is often referred to as "modified Fowler–Nordheim tunneling." In such examples, direct band-to-band tunneling may take place through both oxide and nitride layers as shown. The tunneling probability function Pt gets modified and incorporates direct probability parameters relating to combined probability through both the layers.

Therefore, direct tunneling current is extremely sensitive to thickness of the dielectric and exponentially reduced as thickness of the dielectric increases. Additionally, Jt is dependent on voltage (not on field), and is electrode controlled through De from the above equation on tunnel current density Jt. It should also be noted that in both variations of direct tunneling, charge transport is not sensitive to temperature.

It may be noted in the above examples of both single and dual insulators associated with MIS structures that when the insulator is very thin, and a positive potential Vi is applied on the metal

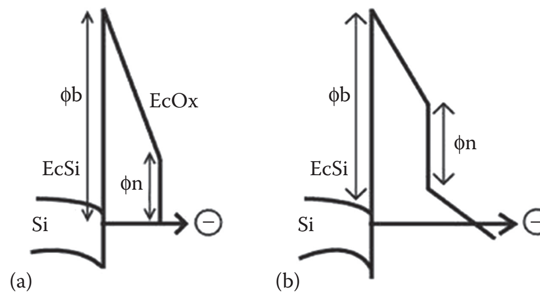

FIGURE 3.5 Quantum mechanical direct tunneling mechanism (electrode controlled): Two related variations: (a) Direct band-to-band tunneling (single insulator) and (b) Modified Fowler–Nordheim tunneling (dual insulator: oxide and nitride).

electrode with Φb > *V*i, electron flows from the silicon conduction band (cathode) across the trapezoidal energy barrier of the insulator or insulators. Correspondingly, current flows from the metal electrode (anode) to the silicon substrate. For example, for oxide (SiO_2) as in case 1.3.5 (a), Φb for electrons is 3.2 eV, direct tunneling mode would be operative in ultrathin oxide in the thickness range of 1–3.2 nm when an external potential is imposed of <3.2 V for a MOS structure.

It should be noted that direct tunneling is ballistic since no scattering of electrons takes place within the insulating film until after the electrons enter the anode. Additionally, current *J*t is not temperature dependent unlike Poole–Frenkel transport. However, as stated earlier, a weak temperature dependence could be observed at low field for silicon-rich insulators where charges are transported from trap to trap by direct tunneling (trap-assisted direct tunneling or resonant tunneling). Another example of such tunneling could be observed in MIS structures when the insulator consists of embedded silicon nanodots sandwiched between two ultrathin oxide films. Electrons tunnel by direct quantum mechanical tunneling first between silicon electrode to the Si-nano dot induced trapping energy states and then from such energy states to the metal electrode. This book will discuss NVM devices based on such transport in section on Direct Tunnel Memories and in section on advanced devices. Many CT devices are also based on direct tunneling of electrons and holes.

3.5.3.1 Fowler–Nordheim Tunneling

When the external voltage across the MIS structure is greater than the energy barriers associated with electrons and holes and the insulator is relatively thicker, charge transport by tunneling takes place through the triangular energy barrier created by the external potential. This is shown in Figure 3.6a; the charged carrier transport mode is known as Fowler–Nordheim tunneling. In this mode of tunneling, the current density J is proportional to the square of the field Ei and is more strongly sensitive to the barrier height Φ_b. The current density Ji is given by:

$$Ji = C\ Ei^2 \exp(-B/Ei)$$

Where C is a Fowler–Nordheim constant related to: (a) electronic charge, *q*; (b) probability parameters, Φ_b; and (c) effective mass, m*; of electrons or holes for the insulator. The parameter, B is proportional to: $m^{*0.5}$. $\Phi_b^{1.5}$. It should be noted that the transport of carriers and associated current flow is strongly sensitive to the field across the insulator, thereby modulating the characteristics of the triangular energy barrier. In recent FG and CT devices, Fowler–Nordheim tunneling mode or modified Fowler–Nordheim tunneling modes had been the primary mode of charge transport through the tunneling layers of the devices.

Fowler–Nordheim tunneling could be ballistic FN when Vd is in the range of 3–9 V and steady-state FN when Vd is greater than 9 V. This has significance in energy transfer and trap-generation within the insulating layer [2], covered in the next section.

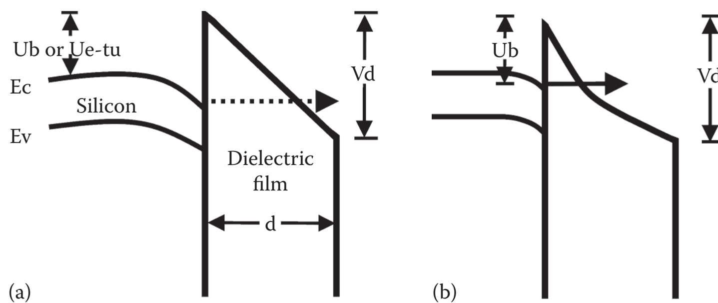

FIGURE 3.6 Fowler–Nordheim tunneling exhibiting triangular energy barrier: (a) Normal or modified Fowler–Nordheim tunneling and (b) Enhanced Fowler–Nordheim tunneling.

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3.5.3.2 Enhanced Fowler–Nordheim Tunneling

An enhanced Fowler–Nordheim mode of current transport is created for thicker dielectric films when the electrode interface provides local high field by effectively modifying and lowering the barrier height Φb (or Ub). Such conditions are created by providing textured polysilicon interface and SRI interfaces with high density of silicon nanodots (injector SRI). The modification of the Fowler–Nordheim triangular barrier is schematically shown in Figure 3.6b. Due to such internal field enhancement, both the effective barrier height as well as the effective tunnel distance could be reduced resulting in enhanced charge transport and current flow for the same insulator thickness. The enhancement current density Ji (enh) could be expressed similar to the above Fowler–Nordheim expression by modifying the term *B* to *B* (enh) as follows:

$$Ji(enh) = C\, Ei^2 \exp[-B(enh)/Ei]$$

Where B(enh) is a function of Φb(enh) is the reduced barrier height as shown in Figure 3.6b. Current density versus gate voltage characteristics for thin oxide MOS devices covering the thickness ranges of 2.5 (direct tunneling) to 7.5 nm (Fowler–Nordheim tunneling) is shown in Figure 3.7 [2,3]. It should be noted that current density through oxide is enhanced by several orders of magnitude at relatively low voltage when charge transport is operating in direct tunnel mode compared to that of Fowler–Nordheim mode.

Examples of enhanced Fowler–Nordheim mode of charge transport in oxide films had been demonstrated by D. DeMaria et al. [3] and shown in Figure 3.8a–c. A thin film of SRO with silicon nanodots was deposited on top of the SiO_2 film in the MIS structure (Figure 3.8a); corresponding modification of the oxide conduction energy band is depicted in Figure 3.8b. Figure 3.8c compares the current–voltage plots with and without interface modification due to the SRO film. Current enhancement of nearly three orders of magnitude due to enhanced Fowler–Nordheim transport mode was demonstrated.

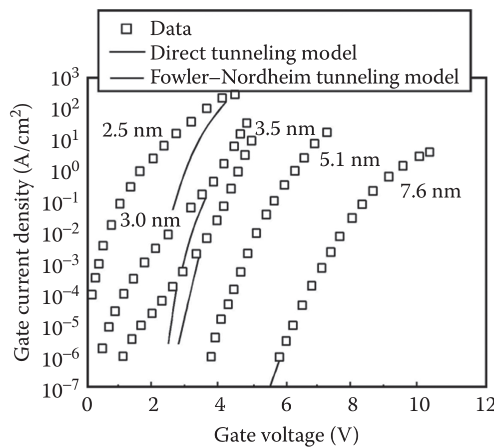

FIGURE 3.7 Current–voltage characteristics in SiO_2 films with both direct tunneling and Fowler–Nordheim tunneling. (From Hu, C., Gate oxide scaling limits and projection, *IEDM*, p. 319 © 1996 IEEE.)

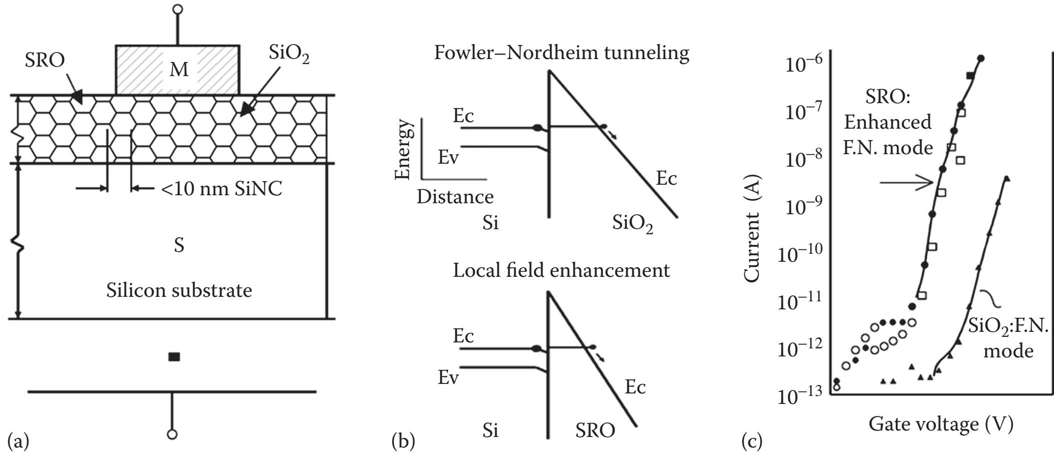

FIGURE 3.8 (a) Enhanced charge injection into SiO_2 due to silicon nanocrystals of silicon-rich oxide (SRO) over layer, (b) Conduction energy band modification associated with silicon nanodots, and (c) Enhanced F.N. current due to the silicon-rich-oxide. (From DeMaria, D. J. et al., *J. Appl. Phys.*, 51, 4830, © 1980 IEEE.)

3.6 CARRIER TRANSPORT MECHANISMS FOR MULTILAYER DIELECTRICS

Advanced NVM devices employ multilayers of dielectric films for tunneling layers and blocking layers. Multilayered trapping dielectric structures have also been suggested to enhance charge retention. Forward and reverse charge transport characteristics could be significantly modified by band-engineered multidielectric gate stack structures for NVM devices. If the dielectric layers are relatively trap-free, charge transport could be characterized in terms of multiple direct tunneling mode or by modified Fowler–Nordheim tunneling mode assuming trapping and detrapping are not involved. Multilayered dielectric structures and related characteristics will be discussed in chapter on band engineering in considerable detail in Part II. In general, transport characteristics in multilayered dielectric structures are modeled by a combination of the different modes outlined above.

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